Software Project/Tarkvara Projekt

# Requirements

Programming languages:

* Java – understanding of basic principles of object oriented programming and test driven development.
* VHDL – basic knowledge of synthesizable subset of VHDL constructs and simulation-only subset to prepare testbenches for simple functional verification.

# Task

The goal of the project is to develop a software for generating a hardware description in the form of structural VHDL code and testbenches for functional verification of generated designs.

The software should elaborate the data model given as input and create a VHDL source files out of this model. The data model itself is not part of this project and will be given as the library of Java classes.

Key challenge: software should be able to handle large amount of data, since it is intended to be part of industrial application.

After completing the project students will acquire basic knowledge of how the industrial application is developed and what are the needs and the challenges.

Supervisors:

Anton Tsertov and Dmitri Mihhailov, both are with Testonica Lab Company and are members of Computer Science department. Anton and Dmitri have more than 10 years of experience in development of commercial application for Worlds leading companies in the field of hardware testing.