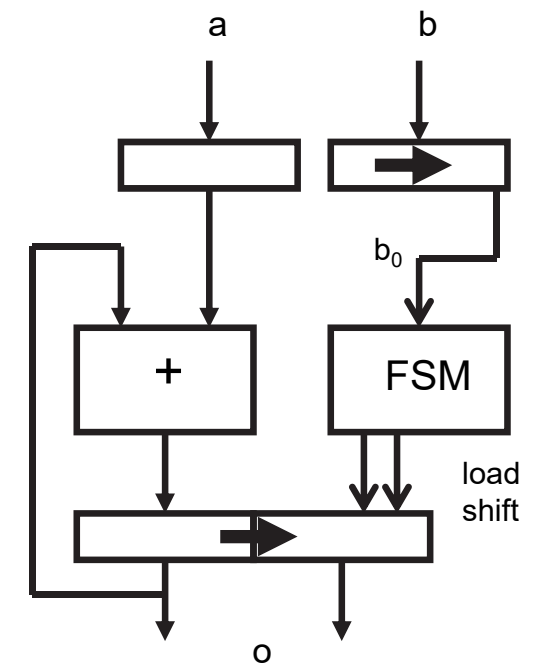


Korrutamisalgoritmid

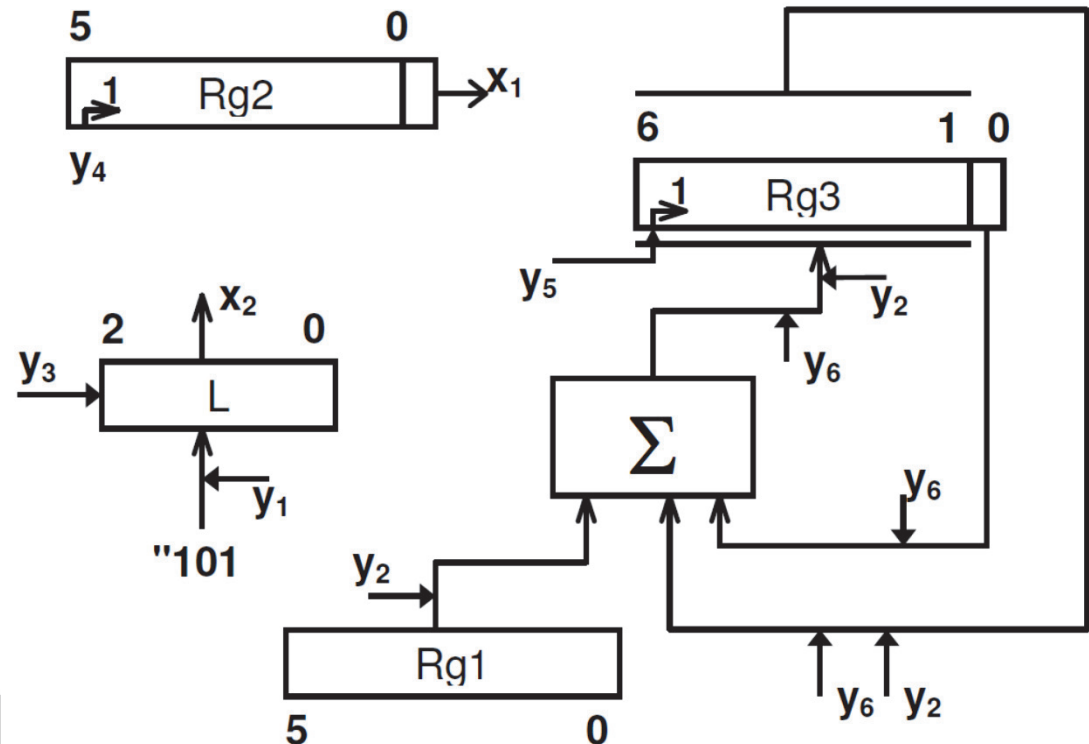
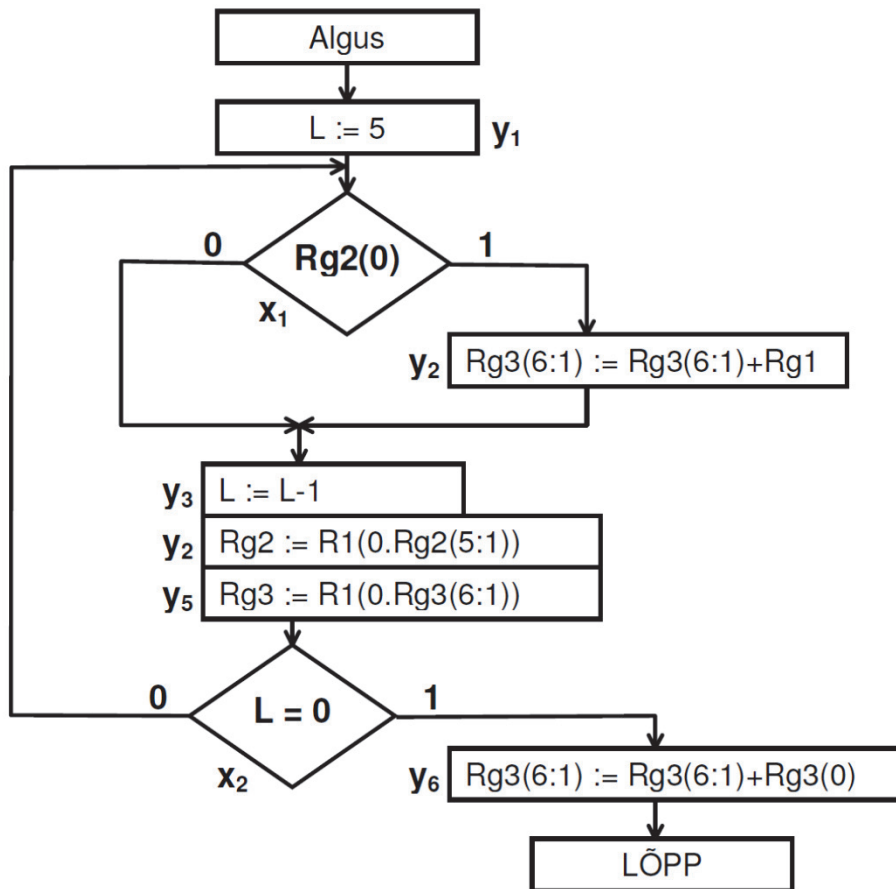
- 2-nd arvude korrutamine
 - analoogne 10-nd arvude korrutamisele

13 * 24	00001101 * 00011000
-----	-----
52	00001101...
26	00001101
-----	-----
312	000100111000



- Liitmine ja nihutamine
- Enamus arhitektuure põhineb sellel algoritmil
 - Kiirendusvõtted kombineerivad eri variante

Korrutamisalgoritmid



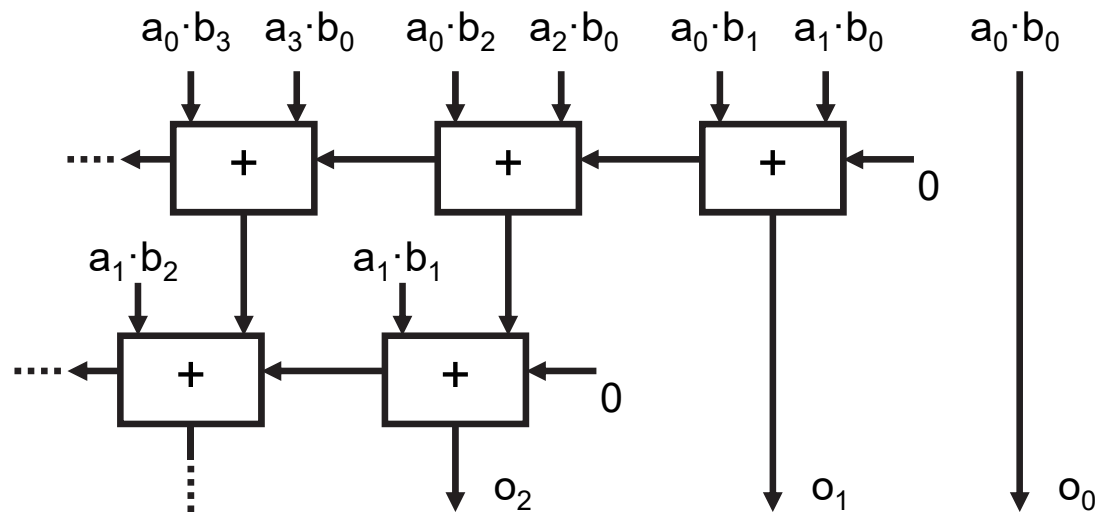
- Margus Kruus – Korrutusalgoritmid

Korrutite arhitektuurid

- Järjestikkorrutid
 - ühe või enama biti kaupa
 - juhtprogramm
 - kiirendamine täiendava analüüsi abil
 - aktiivsete bittide arv
 - kahe biti kaupa (radix-4)
 - $\dots + [0,1,2,3]*a - 3*a = 4*a - a$
 - 32-bitine korrutamine 16-bitiste korrutitega
 - $(a_H*2^{16}+a_L) * (b_H*2^{16}+b_L) =$
 $a_H*b_H*2^{32} + a_H*b_L*2^{16} + a_L*b_H*2^{16} + a_L*b_L$

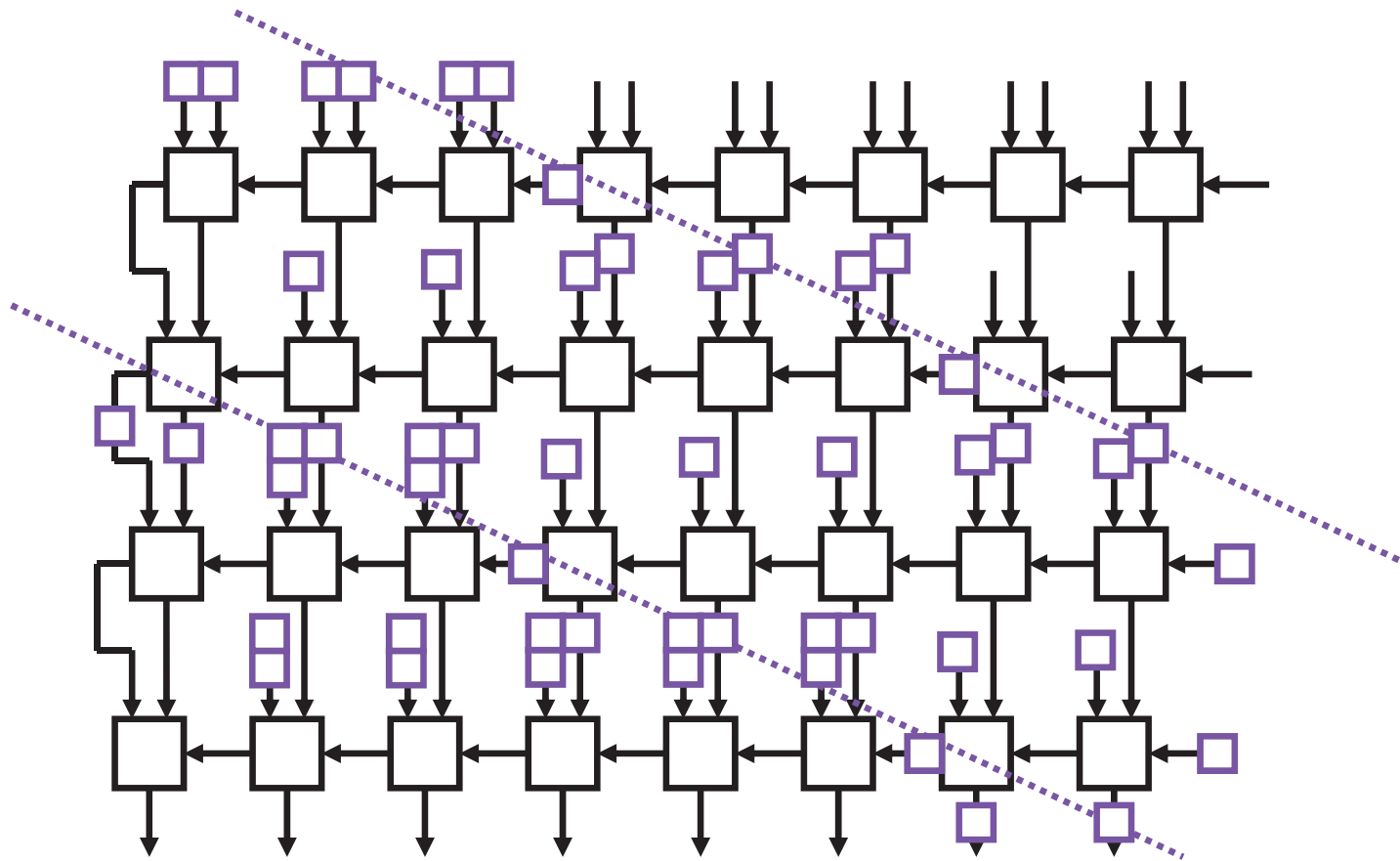
Korrutite arhitektuurid

- Paralleelkorrutid
 - matrikskorruti
 - AND tehe ja täissummaator
 - konveierkorruti – registrid matriksis



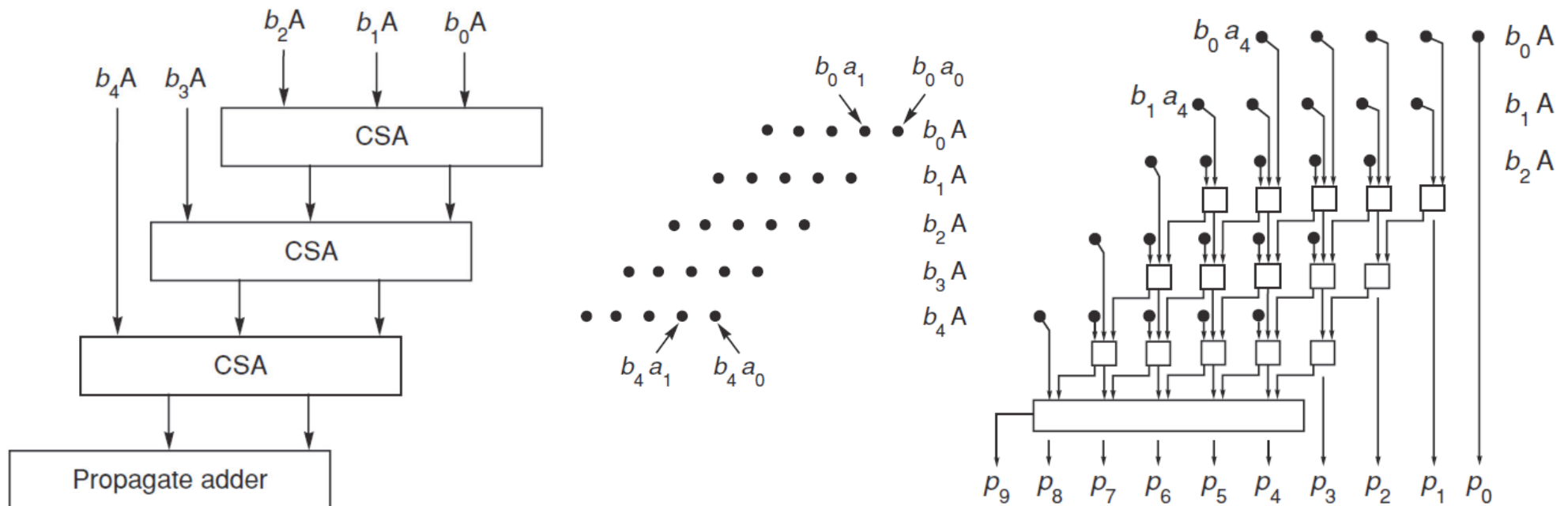
Korrutite arhitektuurid

- Konveierkorrupti – registrid matriksis

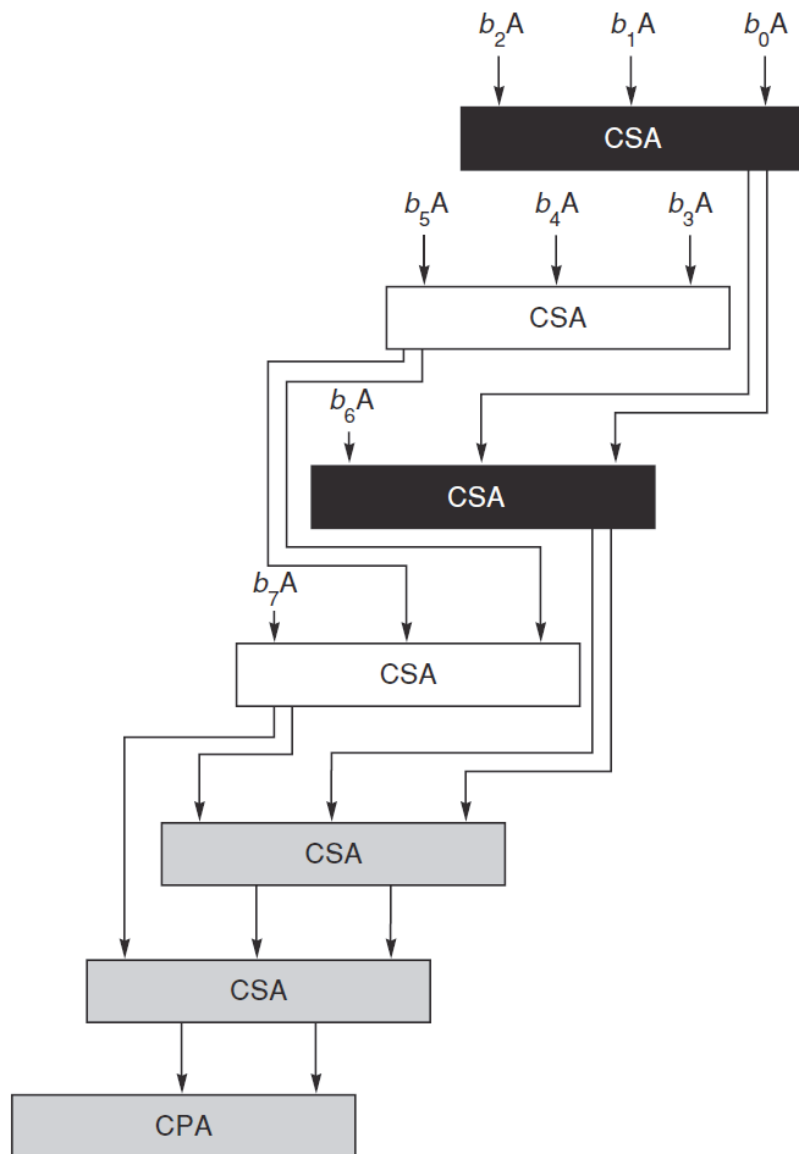


Korrutamise kiirendamine

- Hennessy & Patterson, Computer Architecture
 - Appendix I – D. Goldberg, Computer Arithmetic



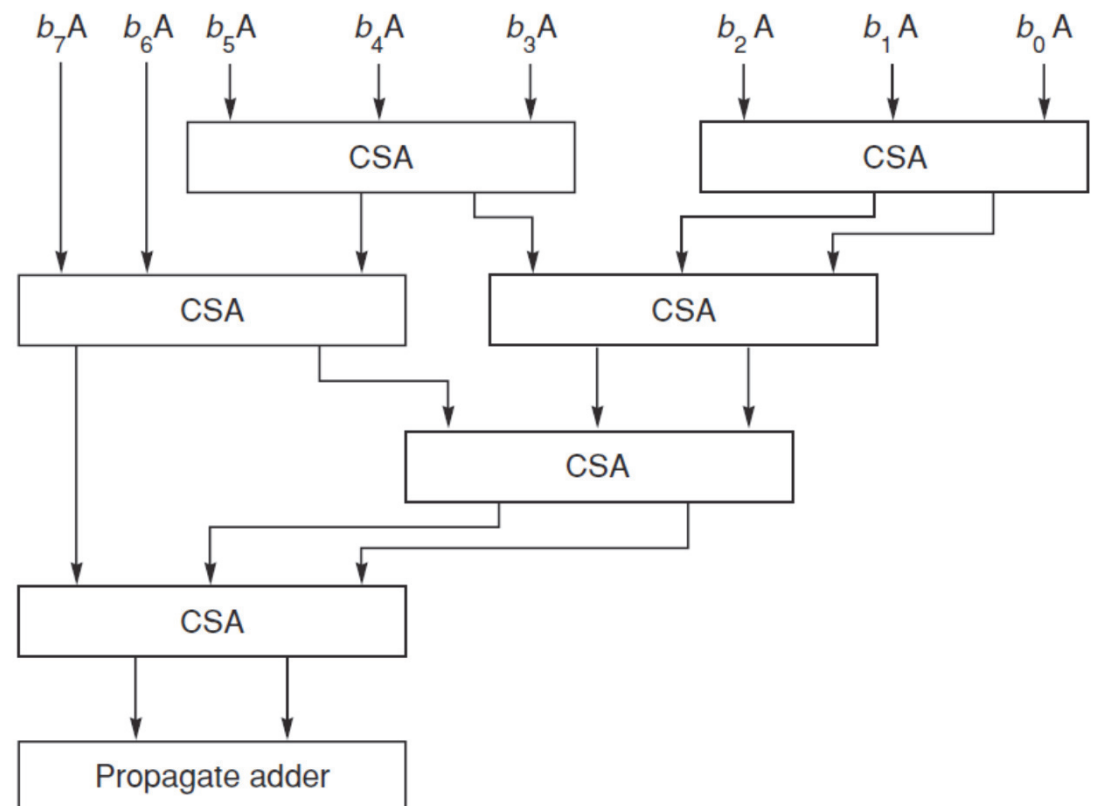
Korrutamise kiirendamine



even/odd array

CSA – carry-select adder

Wallace tree



Aritmeetikatehete simulaator

<http://www.ecs.umass.edu/ece/koren/arith/simulator/>

2's Complement Array Multiplier

A: 00101
X: 11001
bin ☐ dec ☒
Number of Bits (>2): 5

Signal Delays

A _i to C _{i+1}	1.5	C _i to C _{i+1}	1.0
C _i to S _i	1.5	A _i to S _i	2.0

Compute
Reset
Help

Booth's Algorithm

A: 15
X: -4
bin ☐ dec ☒
Number of bits: 8
Compute

A 00101 : 5
X x11001 : -7
Product 1111011101 : -35
Total Delay for Multiplier = 12

A	00001111	15
X	x11111100	-4
Y	00000-100	recoded multiplier

Shift Only	000000000
Shift Only	000000000
Add -A	+11110001

	1111000100
Shift	11111000100
Shift Only	111111000100
Shift Only	1111111000100
Shift Only	11111111000100
Shift Only	111111111000100
Shift Only	1111111111000100 -60