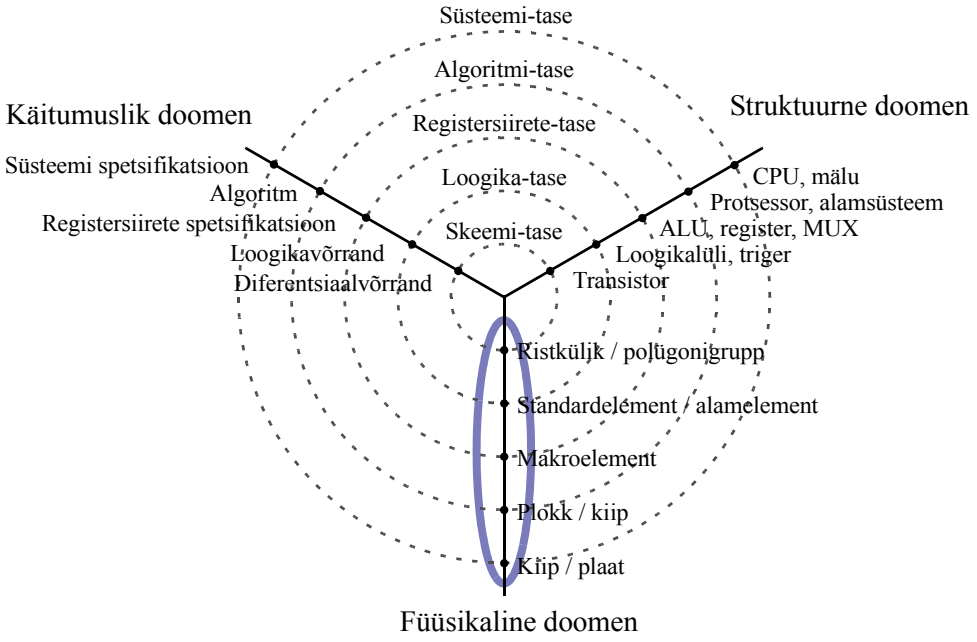
Disaini põhietapid

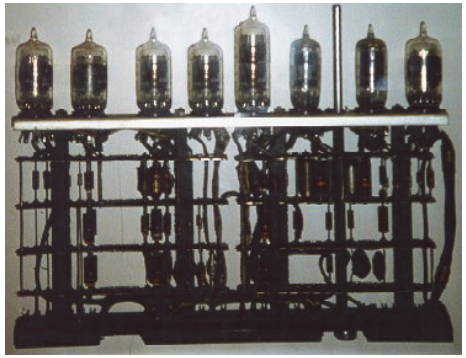
- **Süsteemi disain - System design**
  a.k.a. **Arhitektuuri süntees - Architectural-level synthesis**
  - **kirjeldus / spetsifikatsioon –> plokk-skeem**
  - **makroskoopilise struktuuri määramine** *ehk*
    kuidas on peamised ühendusplokid omavahel ühendatud

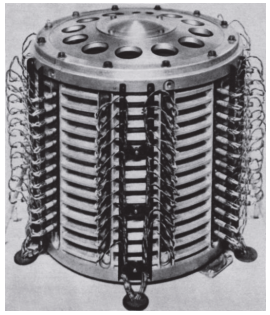
- **Loogikadisain - Logic Design**
  - **plokk-skeem –> loogikalülid**
  - **mikroskoopilise struktuuri määramine** *ehk*
    kuidas on loogikalülid omavahel ühendatud

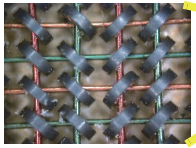
- **Füüsiline disain - Physical design**
  a.k.a. **Geomeetria süntees - Geometrical-level synthesis**
  - **loogikalülid –> transistorid, ühendusjuhtmed, mikroskeem**

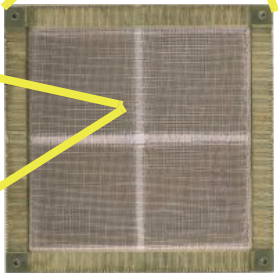


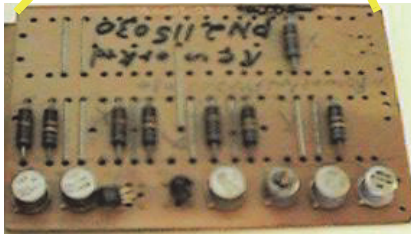
Füüsiline realiseerimine – ajalugu ja tänapäev

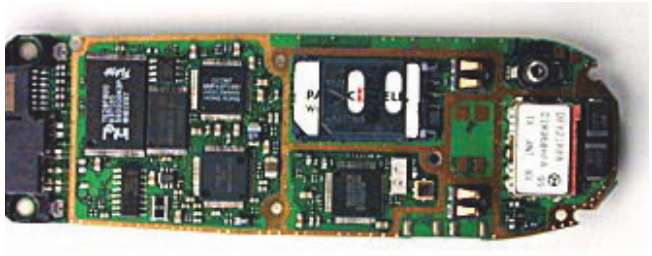






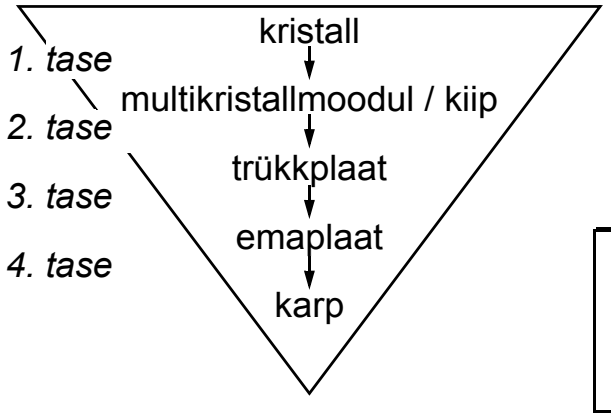


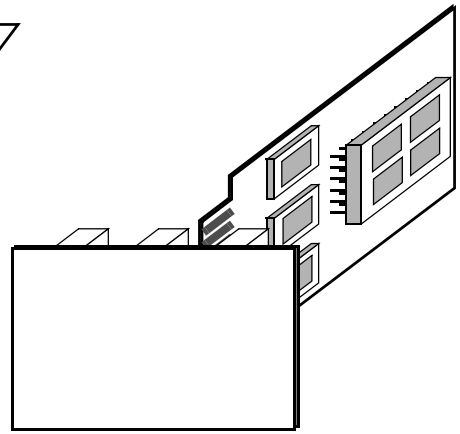




Pakendamine

- **Pakendamise hierarhia**
  - **Lahendatavad ülesanded**
    - **elektrilised**
    - **mehhaanilised**
    - **termilised**

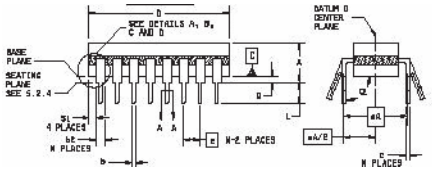


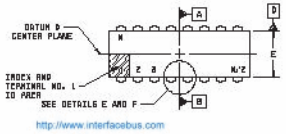


- **Kiipide/korpuste tüübid**
  - **Aukmonteeritavad (läbi trükkplaadi)**
    - **DIP: Dual In-line Package; PGA: Pin Grid Array**
    - **C-DIP, CERDIP, CPGA, TBD, HDIP, PDIP, PPGA, Shrink DIP, SIP**
  - **Pindmonteeritavad**
    - **PLCC: Plastic Leaded Chip Carrier; SOIC: Small Outline IC; BGA: Ball Grid Array**
    - **BQFP, CBGA, CFP, CPGA, CQFP, TBD, DLCC, FBGA, fpBGA, JLCC, LCC, LCCC, LFBGA, LGA, MLCC, PBGA, PQFD, PQFP, PSOP, QFP, QSOP, SOJ, SSOP, TQFP, TSOP, TSSOP, TVSOP, VQFB**
  - **http://www.interfacebus.com/Design_Pack_types.html**

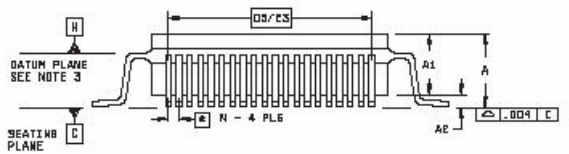
Kiipide/korpuste näited

DIP

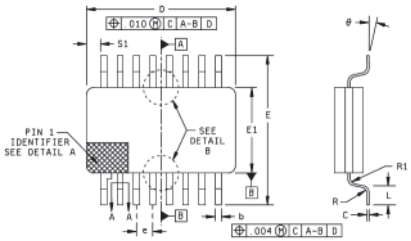




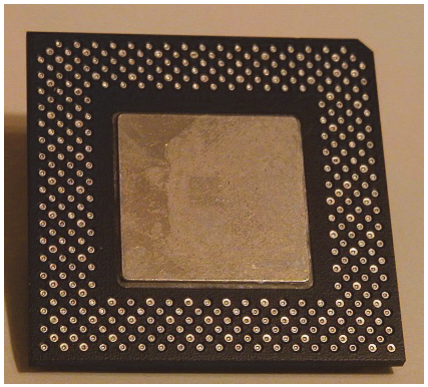
PLCC



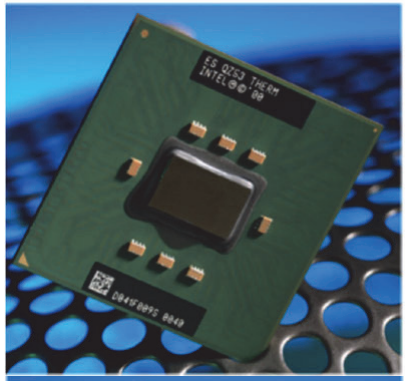
SOIC

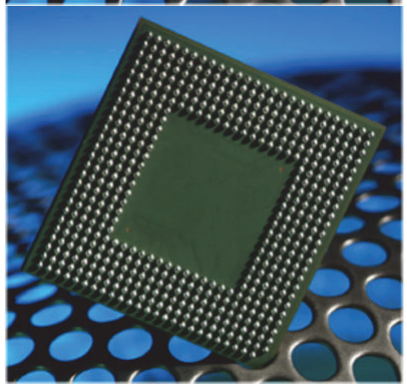


PPGA (Intel)

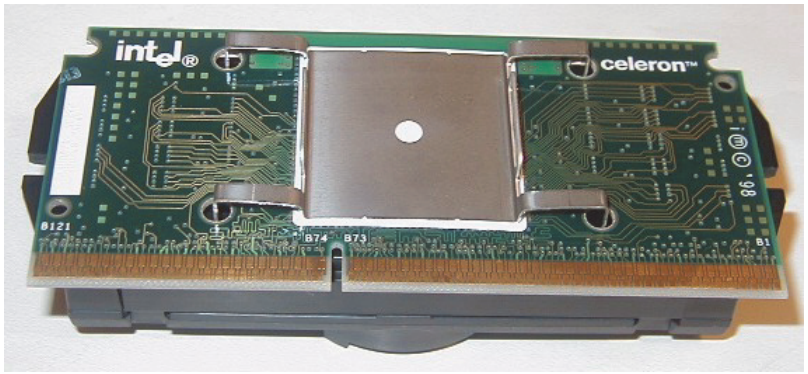


FCBGA (Intel)



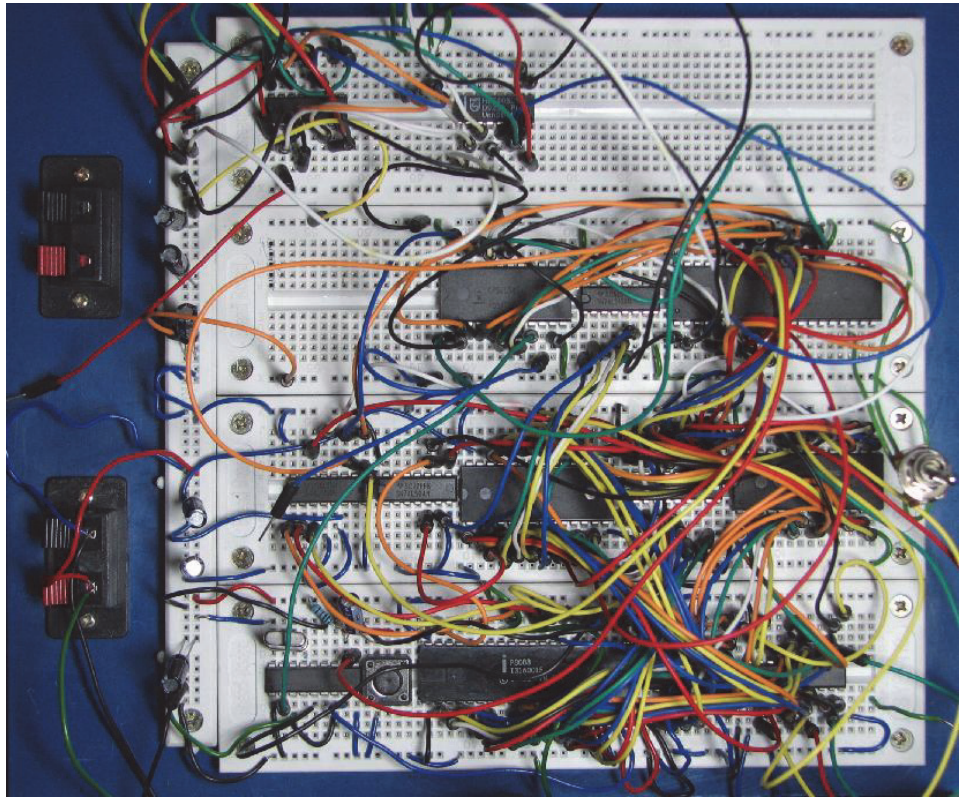


SEPP (Intel)

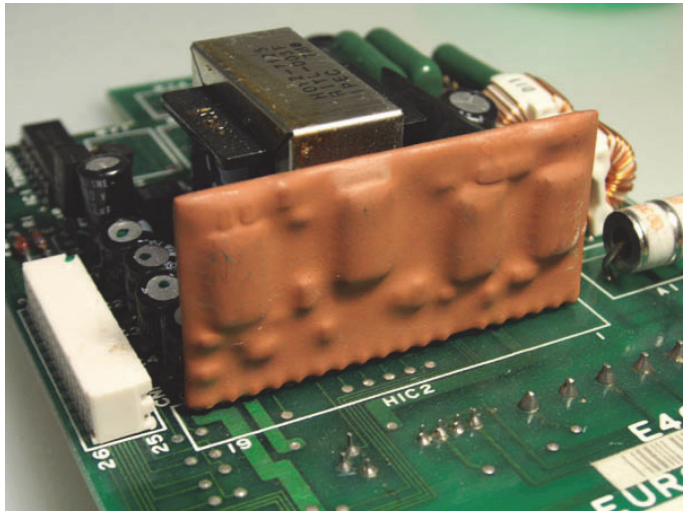


Pakendamise näited

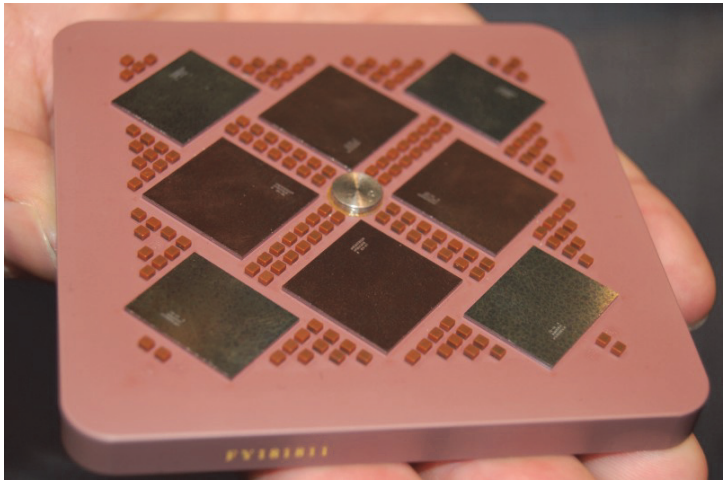
prototüüpimine



hübriidmikroskeem



ruumiline montaaž



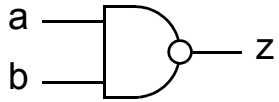
IBM POWER5

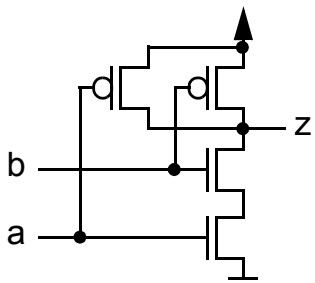
VLSI füüsiline disain

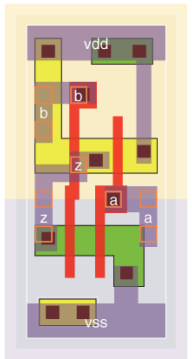
- **Loogika tase**
  - **loogikaelemendid / loogikaavaldised**
  - **ahelad / bitid**
- **Füüsika tase**
  - **transistorid / traadid**
  - **polügonid**

vt. ka http://www.vlsitechnology.org/

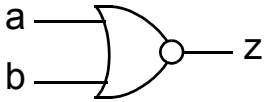
2-NAND

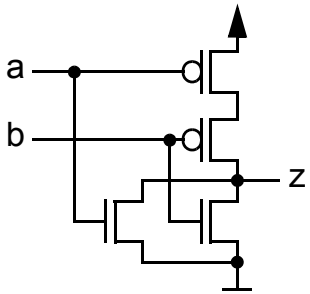


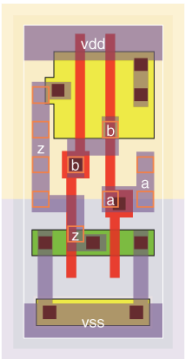




2-NOR







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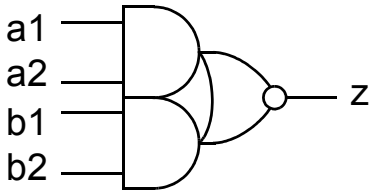
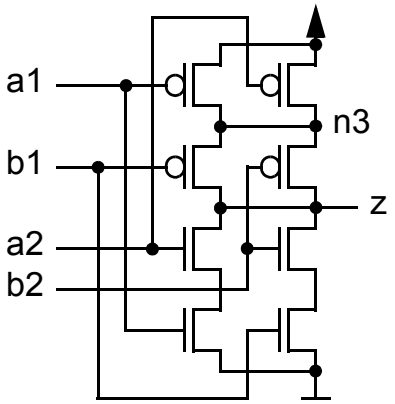
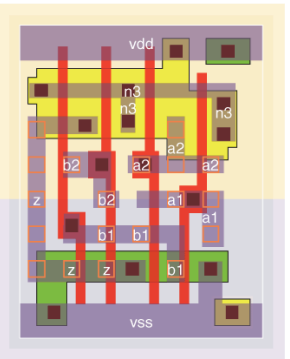
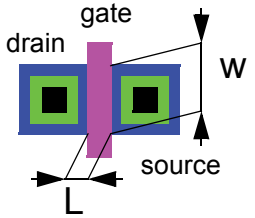


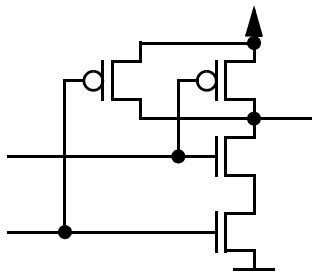


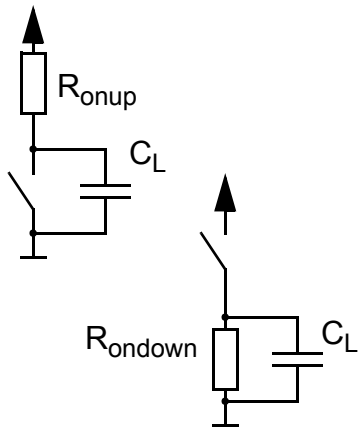


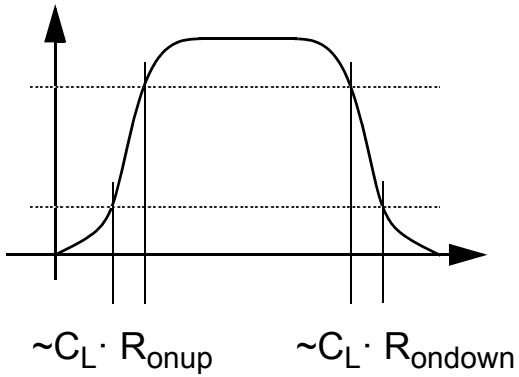
CMOS - miks NAND?

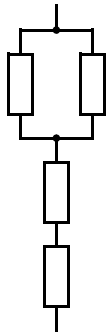
- **Materjalide omadused – <u>mobiilsus</u> –**
  μ_n = 1250 cm^2 / V sec & μ_p = 480 cm^2 / V sec
- **R ~ μ^{-1} & R ~ L w^{-1} (L - konstant)**











$R \sim \mu^{-1} w^{-1}$

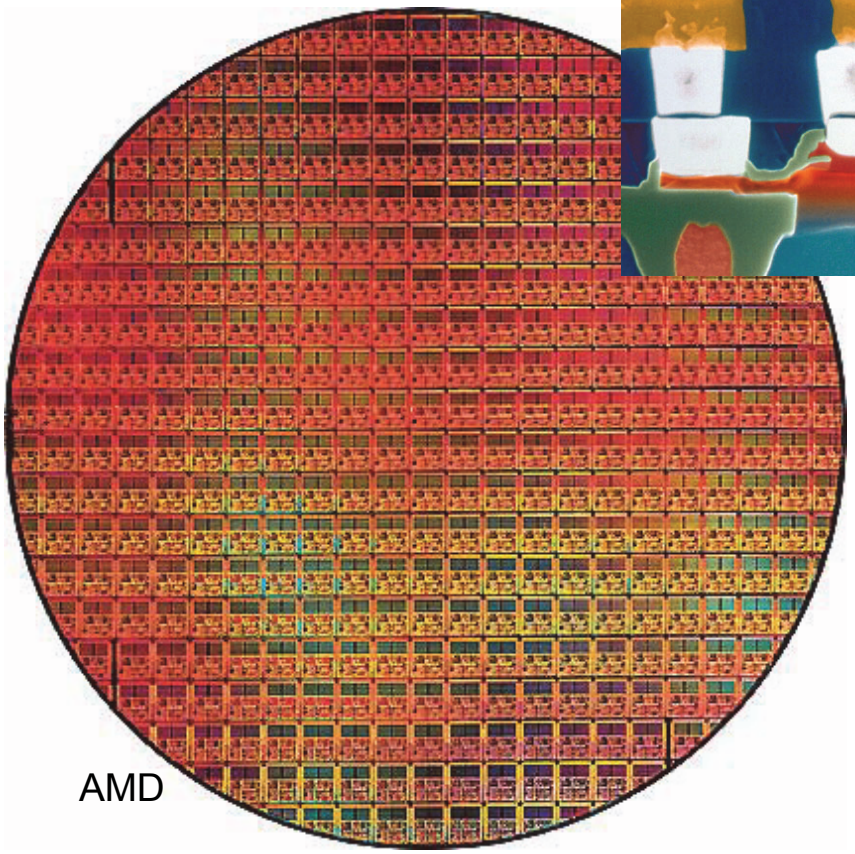
$w_p \sim 3 \cdot w_n \quad (R_p = R_n)$

$R_p || R_p \sim R_n + R_n$

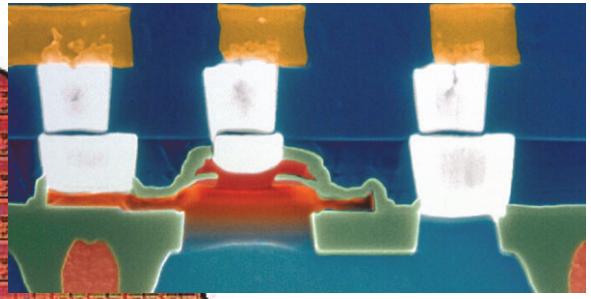
$R_p \sim 4 \cdot R_n \quad (w_p = w_n)$

Mikroskeemide valmistamine

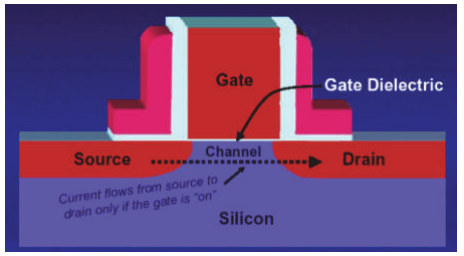
- maskid – ilmutamine
- söövitamine / lisamine
- pakendamine
- testimine

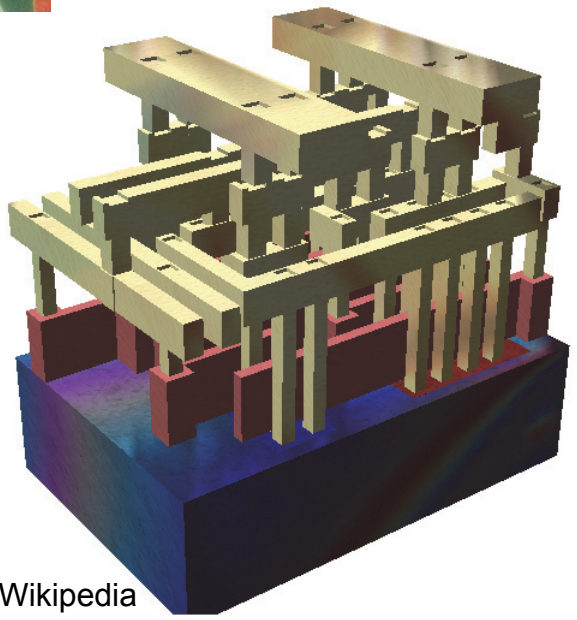

AMD

Brown University



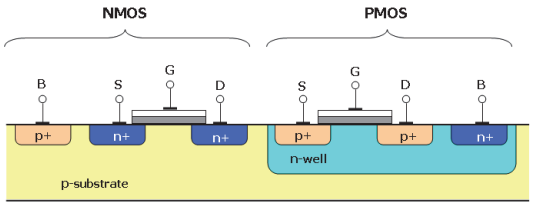
Robert Richmond, 2003




Wikipedia

Protsessi sammud

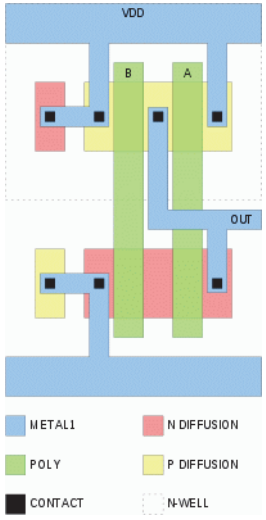
CMOS transistorid



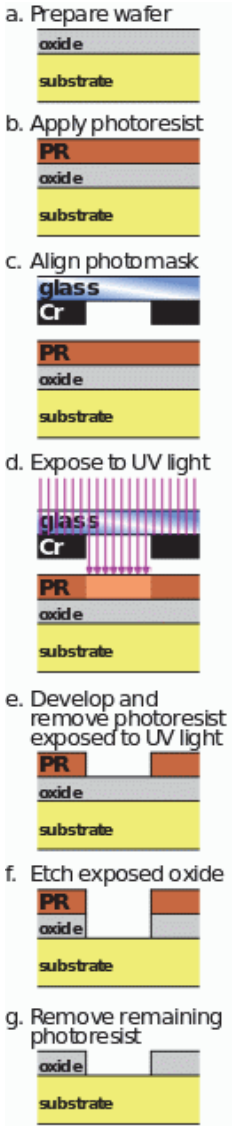
n - elektronid [P, As, Sb]
p - augud [B, Al]

http://jas.eng.buffalo.edu/
CMOS inverter fabrication

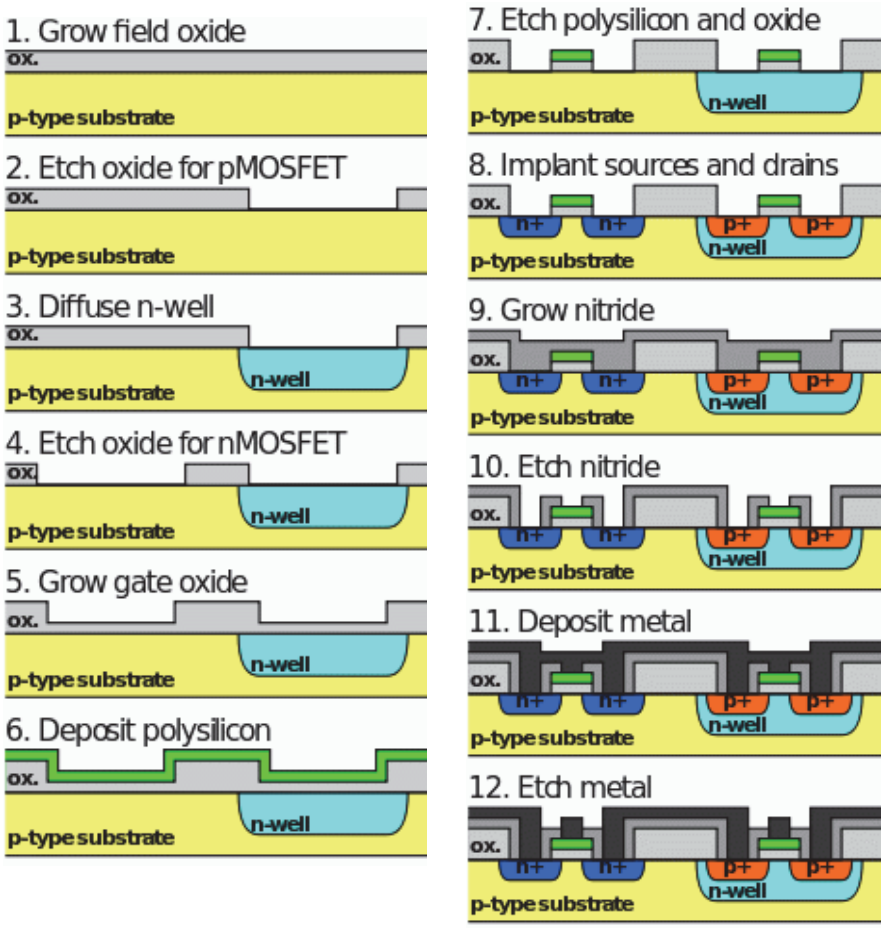
2-NAND pinnalaotus



söövitamise sammud



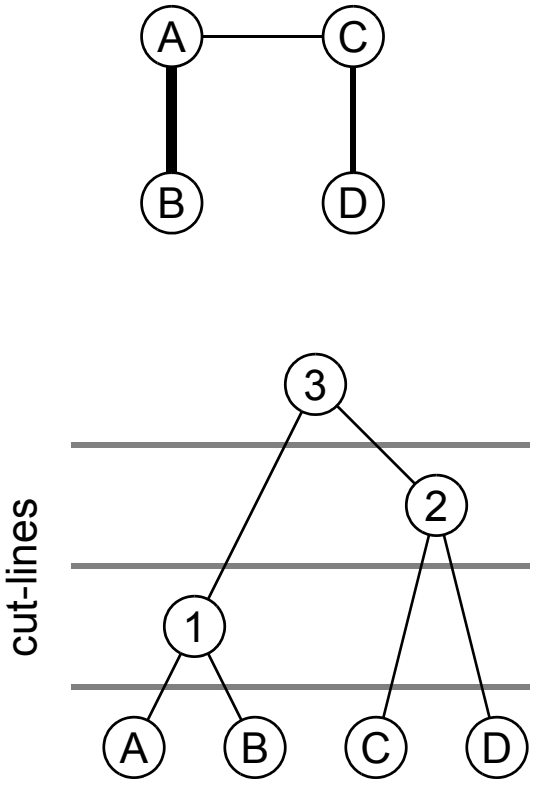
valmistamise sammud



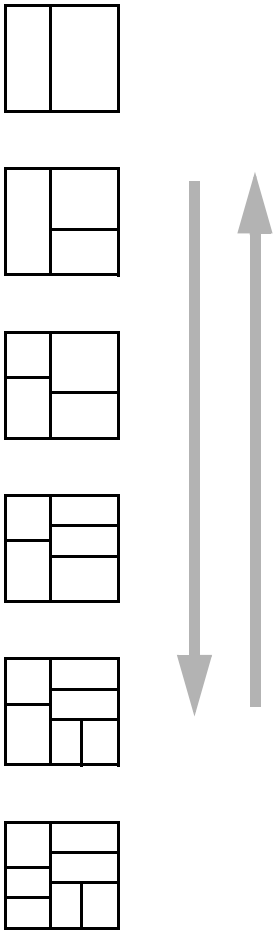
www.wikipedia.org

Pinnalaotuse süntees

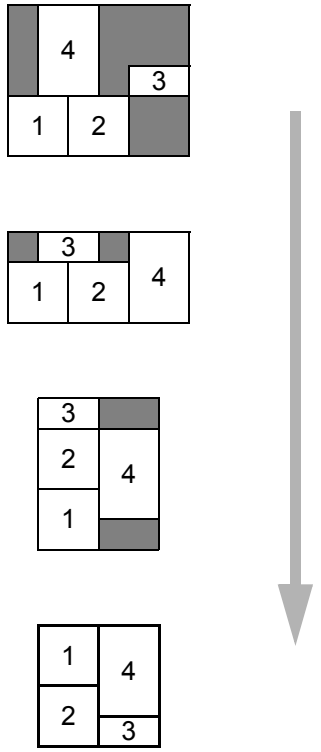
- **Tükeldamine**



- **Pinnaplaneering**



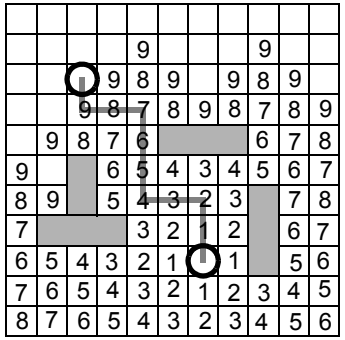
- **Paigaldamine**

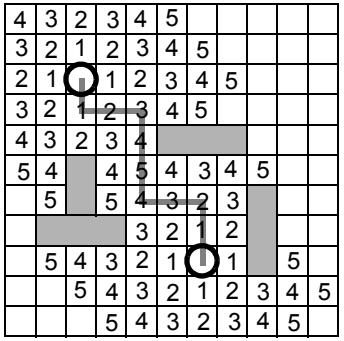


Pinnalaotuse süntees

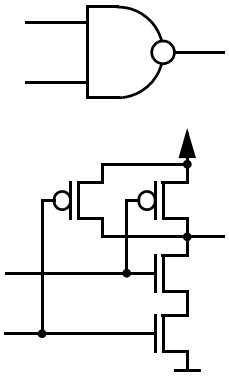
- **Ruutimine (trasseerimine)**
  - **labürindi läbimine**
    - **vajab palju mälu!**
    - **kahesuunaline otsimine**
    - **mitmekihiline ruutimine**

Ruutimine

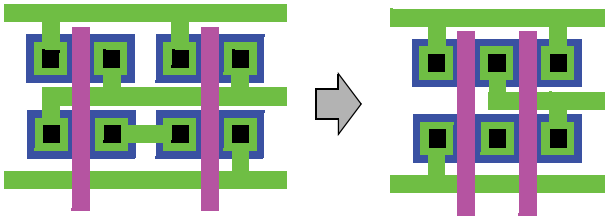




- **Pinnalaotuse optimeerimine**



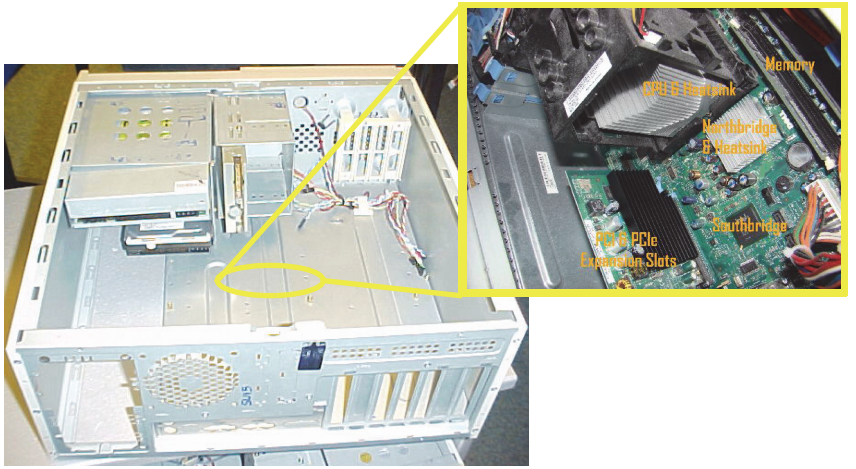
Optimeerimine

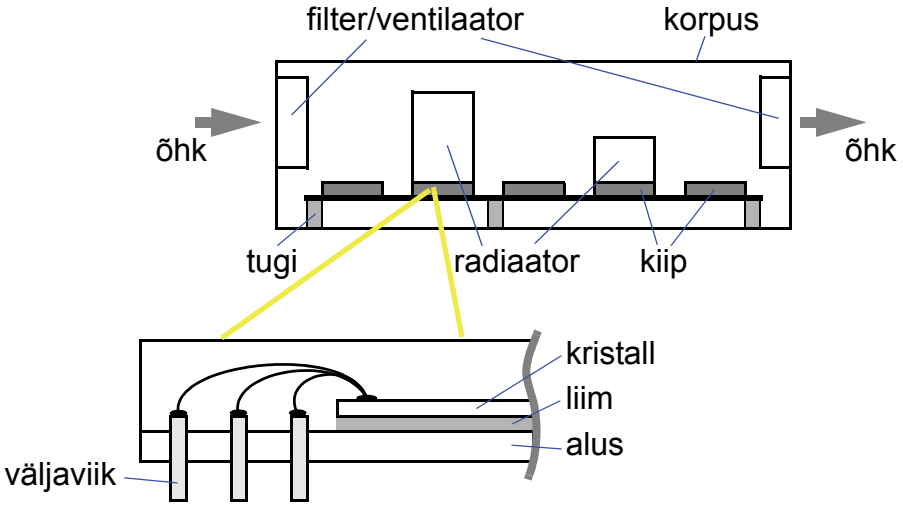


- **Pinnalaotuse kontroll**
  - **DRC (Design Rule Check)**

Pakendamine - korpused

- Füüsilised nõuded ja piirangud
  - mõõtmed, liidesed
  - vastupidavus - tolm, vibratsioon
- Termilised nõuded ja piirangud
  - töötemperatuuri vahemik
  - jahutamine / küte
- Elektrilised nõuded ja piirangud
  - elektritoide
  - kaitse - liigpinge, elektromagnetväljad
- Ergonoomilised nõuded ja piirangud
  - väljanägemine, kasutajaliides, müra

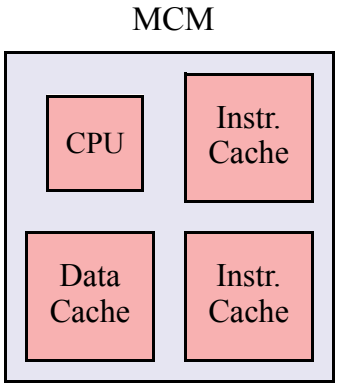


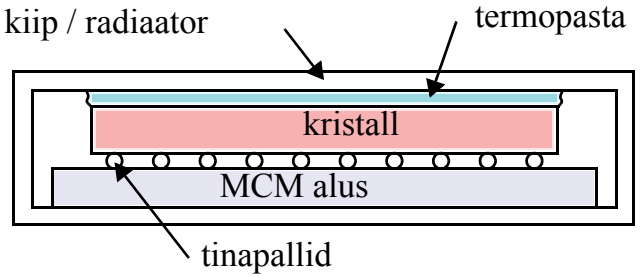


Termilised probleemid

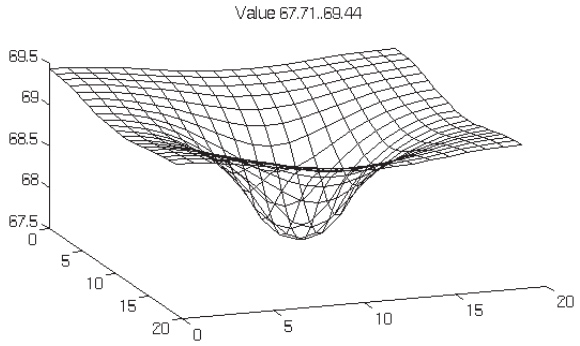
- **Jahutamine**

- **Näidisdisain (MCM)**
  - **CPU - 68 mm^2, cache - 112 mm^2**
  - **koguvõimsus - 72 W**
  - **soojuse eemaldamine**
    - **kristall (GaAs): 46 W/mK**
    - **väljaviigud (tinapallid):**
      ***d* 0.1 mm, samm 0.25 mm, 36 W/mK**
      (CPU 361 & cache 441)
    - **termopasta:**
      paksus 0.2 mm, 1.1 W/mK
    - **MCM alus (alumina):**
      27x27 mm, 20 W/mK
    - **kiip/radiaator (Al): 238 W/mK**

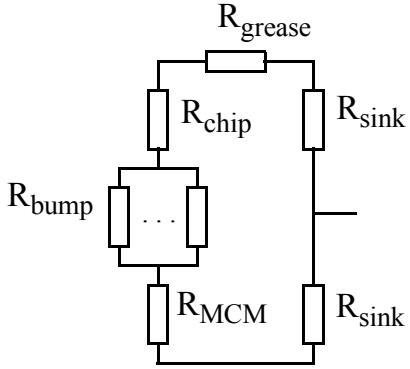




Temperatuuri jaotus väljaviigu ümbruses



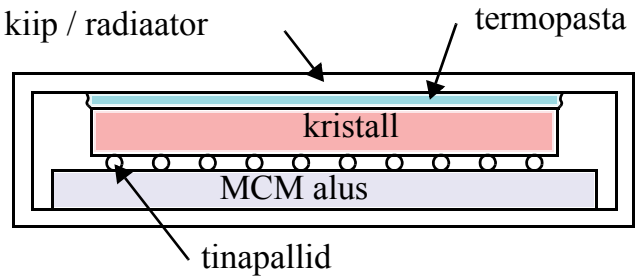
Soojusvoo mudel

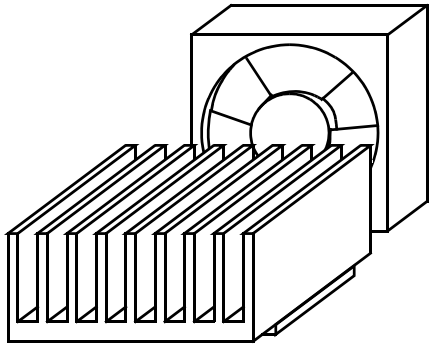


Termilised probleemid

- **Jahutamine (järg)**
  - **temperatuuride vahed**
    - **väljaviik & MCM: 20-25 K**
    - **koos termopastaga: 15-16 K**
  - **radiaator**
    - **vaba õhuvool: 5 W/m^{2}K**
    - **sundjahutus (ventilaator): 50 W/m^{2}K**
    - **kristalli temperatuur $\leq$ 80°C**
    - **radiaatori pindala [cm^2]:**

Radiaatori temperatuur [°C]	Keskkonna temperatuur			
	vaba õhuvool		sundjahutus	
	50°C	30°C	50°C	30°C
64.0	10286	4237	1029	424

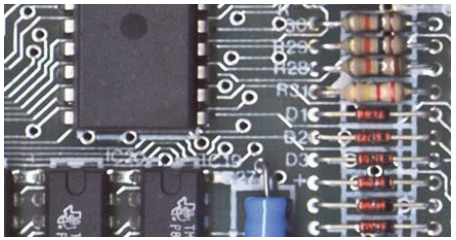




- **Termiline paisumine**
  - **kristall (GaAs): 6.8·10^{-6} K^{-1} (paisub kuni 1.4 μm); MCM alus (alumina): 7.7·10^{-6} K^{-1}**

Trükkplaadid

- PCB (Printed Circuit Board)
- Valmistamine ja projekteerimine
  - töökindlus, maksumus, jõudlus...
  - Komponendid
    - mikroskeemid, transistorid, takistid, kondensaatorid jne.
  - Ühendused
  - Liidesed
  - Kinnitused

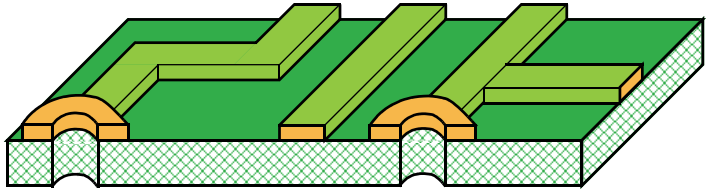


- Trükkplaadi valmistamine
- Komponentide paigaldamine (ja kinnitamine)
- Elektriliste ühenduste loomine (nt. jootmine)

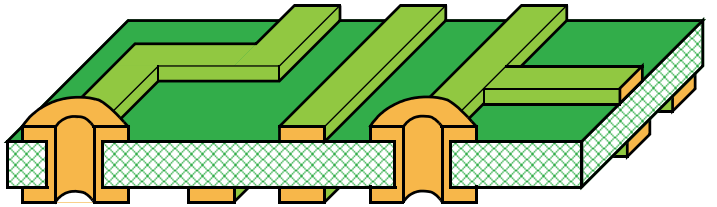
Trükkplaatide valmistamine

- **Vasega (Cu) kaetud tekstoliit (klaasriie+epoksüvaik)**
- **Ühekihiline trükkplaat**
  - **ühendusrajad (alumine pool)**
- **Kahekihiline trükkplaat**
  - **ühendusrajad**
  - **metalliseeritud läbiviigud**
- **Mitmekihiline trükkplaat**
  - **mitu kahekihilist plaati**
  - **läbiviikude asukohad!**

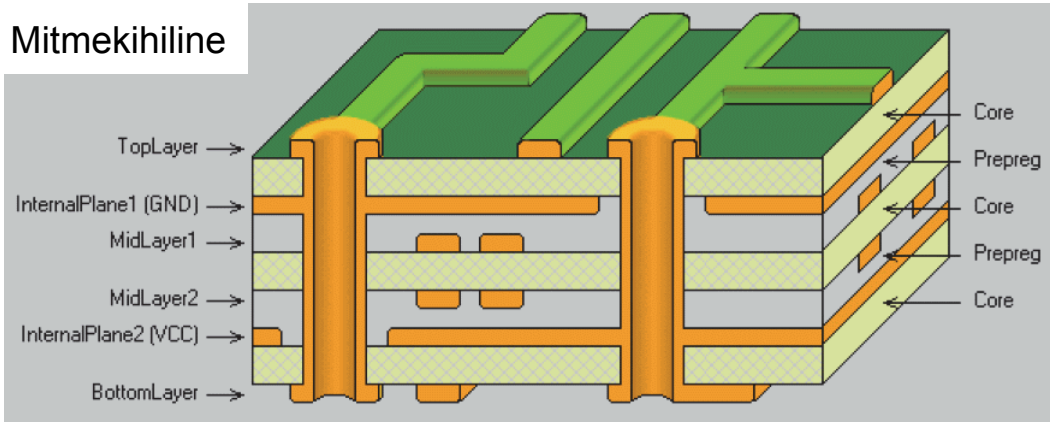
Ühekihiline



Kahekihiline



Mitmekihiline



Trükkplaatide valmistamine

Väikeseeriad / üksikeksemplarid

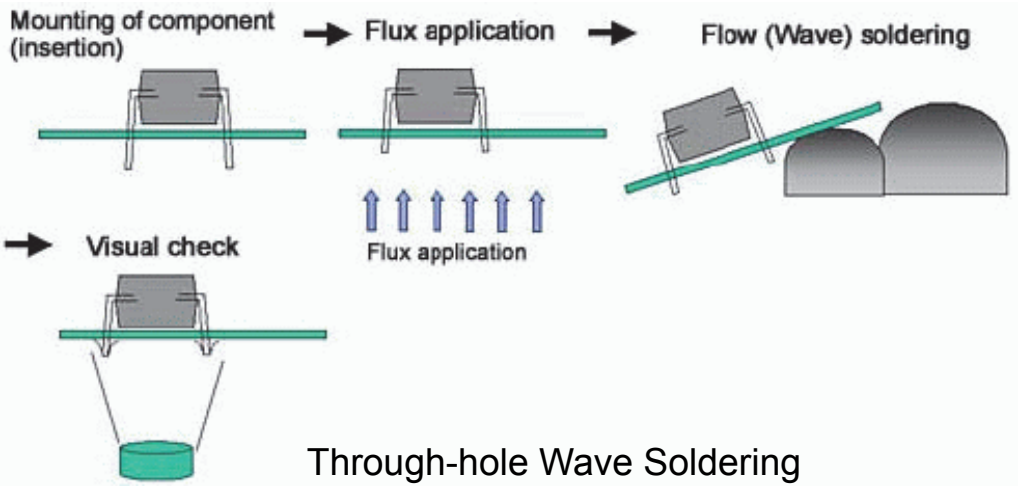
- Täielikult vasega kaetud plaat (1- või 2-kihiline)
- Läbiviikude puurimine (drilling)
- Läbiviikude galvaaniline metalliseerimine
- Ühendusradade loomine == liigse vase eemaldamine
  - liigse metalli söövitamine (etching)
    1) kaitsekihi peale kandmine (radade positiivkujutis)
       a) kaitselaki / -värvi joonistamine / siiditrükk
       b) printimine (fototundlik materjal, termokiled jne.)
    2) söövitamine ($FeCl_3$, HNO_3 jne.)
  - liigse metalli välja freesimine (milling)
- Komponentide paigaldamine
  - vajaduse korral ka kinnitamine (nt. liimimine)
- Jootmine
  - mehhaniseeritud (tinalaine) või käsitsi

Trükkplaatide valmistamine
Suurseeriad

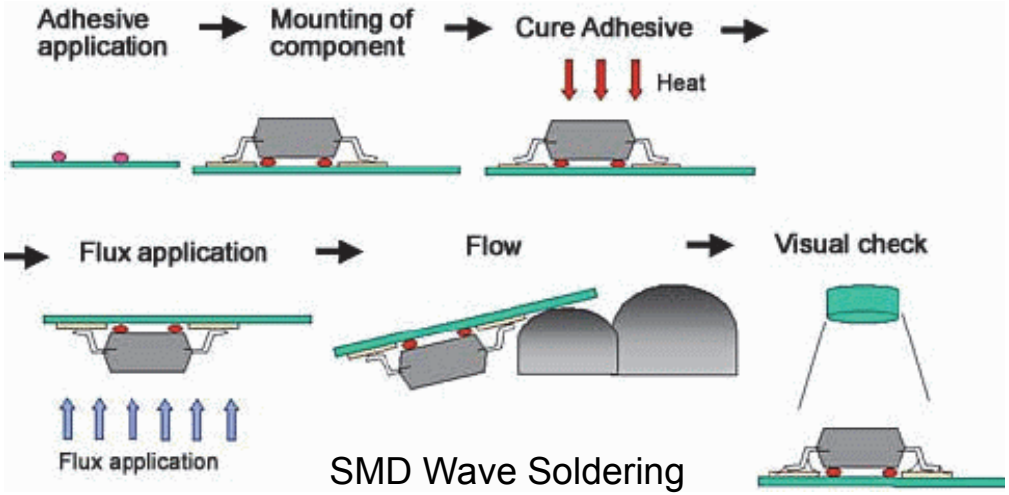
- Läbiviikude puurimine (metalliga katmata plaat)
- Ühendusradade loomine == vasekihi galvaaniline kasvatamine
  - keemiliselt kantakse peale õhuke vasekiht
  - radade asukohtade trükkimine (fotolitograafia)
  - galvaaniline radade kasvatamine vajaliku paksuseni (tagab ka läbiviikude metalliseerimise)
  - liigse vase eemaldamine (söövitamine)
- Kaitsekihi (-laki) ja jootevedeliku/-tinaga katmine
- Komponentide (mehhaniseeritud) paigaldamine
  - vajaduse korral ka kinnitamine (nt. liimimine)
- Jootmine
  - mehhaniseeritud

Trükkplaatide valmistamine

- Valmistamine
  - komponentide kinnitamine
  - jootmine
    - jootevedelik / -tina
  - termilised probleemid
    - suured vasepinnad
    - komponentide ülekuumenemine
  - kvaliteedi kontroll
    - visuaalne
  - lõppviimistlus
    - puhastamine
    - kaitselakkimine
  - lõpptestimine
    - funktsionaalsuse kontroll



Through-hole Wave Soldering



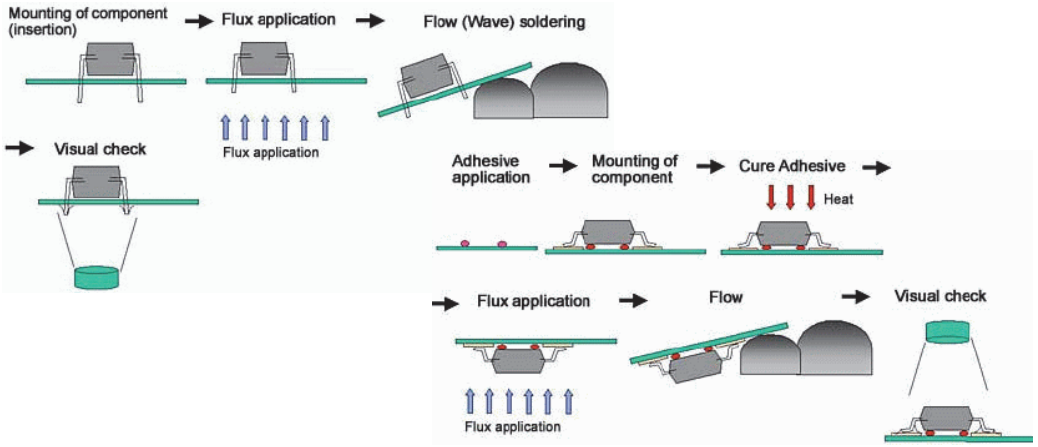
SMD Wave Soldering

Trükkplaatide valmistamine

Wave Soldering

Electro Soft Inc.
https://www.youtube.com/watch?v=inHzaJIE7-4

Agrowtek Inc.
https://www.youtube.com/watch?v=VWH58QrprVc

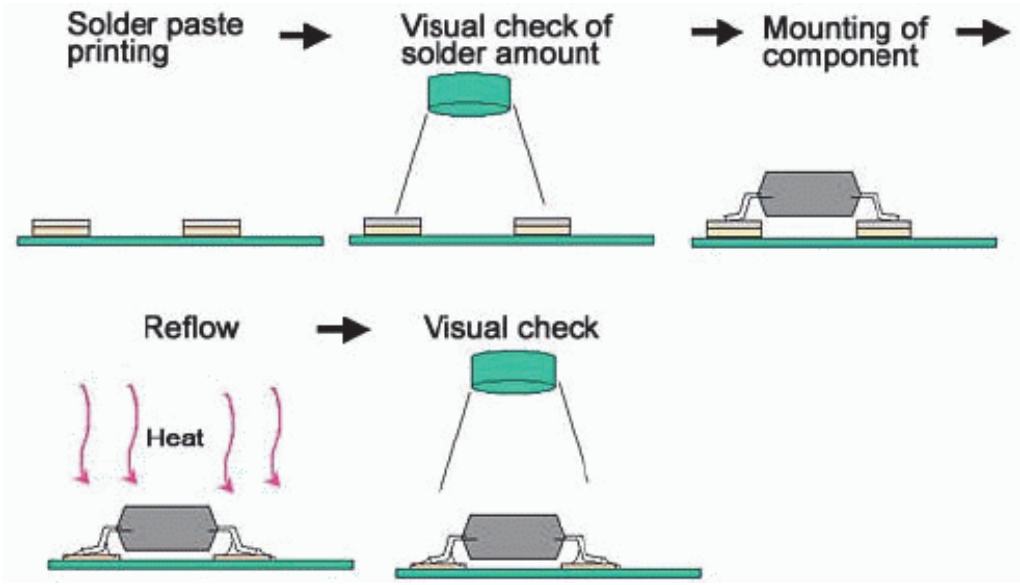


SMD Reflow Soldering

GIGABYTE factory tour
https://www.youtube.com/watch?v=Va3Bfjn4inA

Tutorial
https://www.youtube.com/watch?v=gu0v8lfLcKg

SMD reflow at home
https://www.youtube.com/watch?v=U48Nose31d4



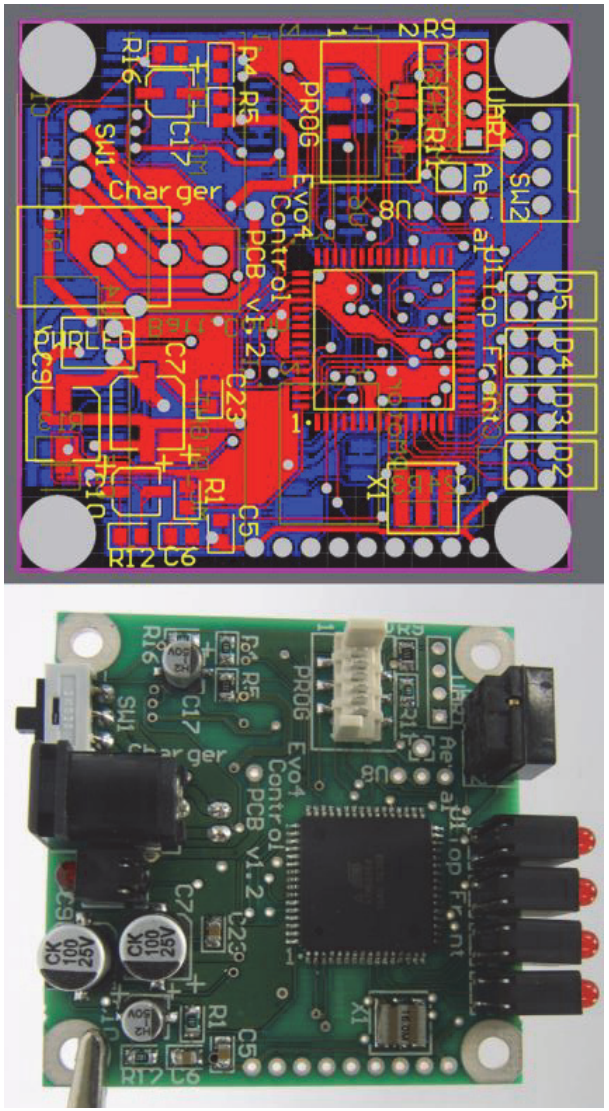
Trükkplaatide valmistamine

Praktilisi nõuandeid

- Mõõtühik on *mil* (1/1000 tolli, st. 0,0254 mm)
- Augud
  - mida väiksem auk, seda kallim plaat
  - väikseimad augud võiksid olla 0,5 mm või suuremd
  - mida paksem plaat, seda suuremad augud – 2 mm plaat -> mitte alla 0,4 mm augud
- Ühendusrajad
  - liiga kitsad rajad ja radadevahed tekitavad probleeme
  - soovitav laius 0,25 mm (10 mil)
- Polügonid (suured pinnad, nt. maakiht)
  - kasutatakse ekraaniks, jahutamiseks jne.
  - väikseim vahe polügoni ja radade vahel vähemalt 0,25 mm
- Jootemask
  - kõikide jooteplatside jaoks peaks olema jootemaskis (kaitselakk) vastav auk
- Markeering
  - ei tohi sattuda jootekohtadele, täpsus ~0,5 mm

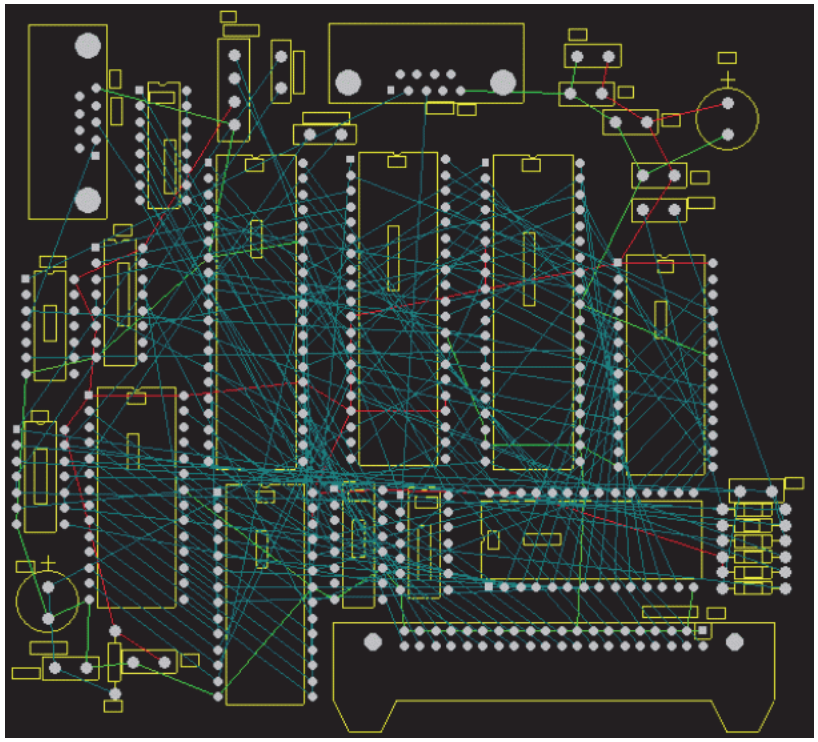
Trükkplaatide projekteerimine

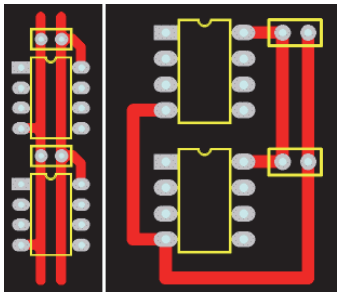
- Skeemist moodulini
  - Skeemi sisestamine
  - Komponentide paigaldamine
    - siinide asukohad
    - tugikomponendid
  - Ruutimine
    - harakapesa (rat-nest) asendamine traatidega
    - toiteühendused
  - Kontroll (DRC)
    - radade mõõtmed
    - radadevahelised kaugused
    - aukudevahelised kaugused
    - jne.



Trükkplaatide projekteerimine

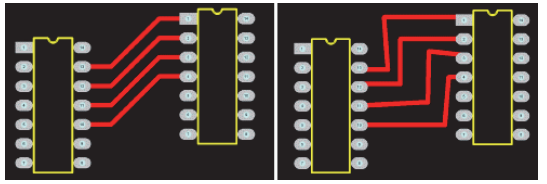
- Projekteerimine
- PCB Design Tutorial
  - David L. Jones
  - http://www.alternatezone.com/
- Mõningaid soovitusi
  - Toite ühendamine
    - filterkondensaatorid
  - Siinide ühendamine
  - Mitmekihilised plaadid
    - läbiviikude tüübid –
      läbi terve plaadi, (osaliselt) peidetud
    - läbiviikude asukohad –
      sünkroniseerimine
- EAGLE
  - Easily Applicable Graphical Layout Editor
  - CadSoft Online – http://www.cadsoft.de/





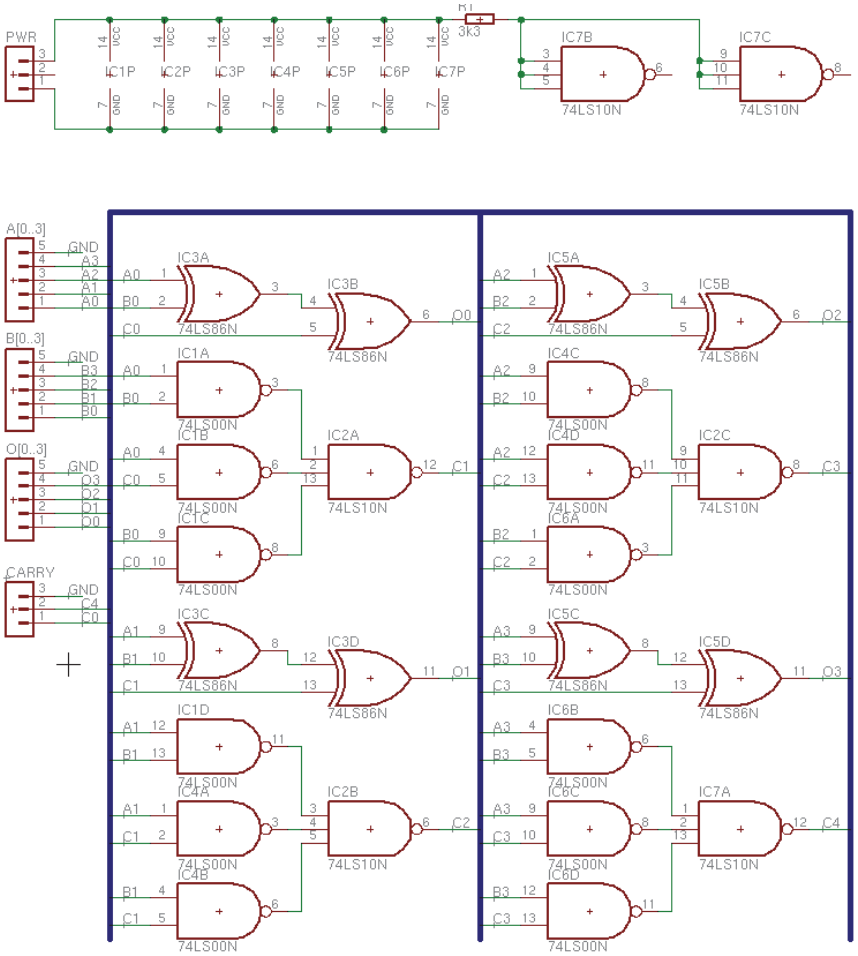
Toide

Siinid

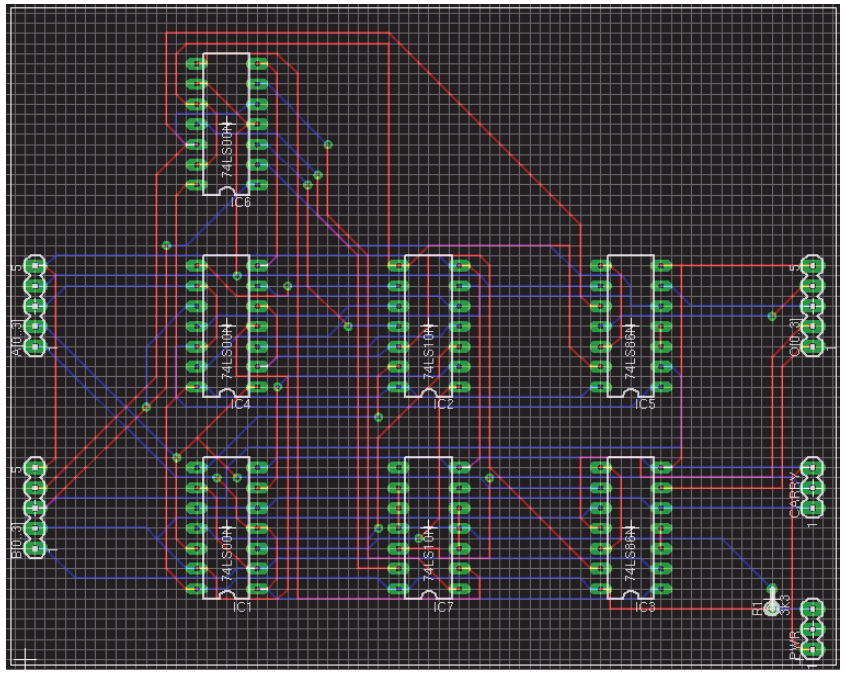


Näidisdisain – 4-bitine summaator

7 kiipi: 2x(4x2-XOR), 3x(4x2-NAND), 2x(3x3-NAND)



36 ahelat, 82 ühendust, 17 läbiviiku



36 ahelat, 82 ühendust, 64 läbiviiku