

BIST Optimization

Choose circuits from Table 1 and constraints from Table 2 according to your variant.
 Example: variant 5 → circuits: C1908, C3540; C1908 constraint – M; C3540 constraint – T

1. Pseudo-random test generation:

- Find out the maximum fault coverage for given circuits applying tuned ATPG.
- Choose “good” seed and polynomial to generate effective pseudo-random test.
- Generated pseudo-random test sequences must have the **maximum fault coverage** and the **length of test** must be in the range $T \leq \text{length} \leq 1,2 * T$ where **T – Time Constraint** from Table 2. (Example: c1908 → 7500 ≤ test length ≤ 9000).
- Use Type I and Type II LFSR generators.

2. Reseeding algorithm:

- Find complete test (max. fault coverage) for given circuit, using the best PRPG (Type I LFSR) test sequence achieved in task 1.
- Perform experiments stepping through the constraint values and **choose 5 results** (test must comply with the constraints specified in your variant). Example: c1908 → M = 1, 2, 3...15 (min. step = 1); T = 7500, 7000, 6500... (min. step = at least 5% of T).

3. Hybrid BIST algorithm:

- Find complete test (max. fault coverage) for given circuit, using the best PRPG (Type I LFSR) test sequence achieved in task 1.
- Perform experiments and choose **5 evenly distributed results** (test must comply with the constraints specified in your variant).

4. Results evaluation:

- According to the marginal results obtained in task 2 and 3 construct the Cost curves on the same graph for Reseeding and Hybrid BIST algorithms.
- Compare results of Reseeding and Hybrid algorithms.

Table 1

| | | | | | | | | | | |
|------------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|
| Variant: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
| Circuits: | C432 | C499 | C1355 | C880 | C1908 | C3540 | S1196 | S1269 | S1423 | S832 |
| | S1196 | S1423 | S832 | S1269 | C3540 | C880 | C499 | C1908 | C432 | C1355 |

Table 2

| <i>Circuits</i> | Time Constraint (patterns): (T) | Memory Constraint (patterns): (M) | α | Cost (C) Constraint $C=T+ \alpha * M$ | Reseeding | | Hybrid BIST | |
|-----------------|---------------------------------|-----------------------------------|----------|---------------------------------------|---------------|----------------|---------------|----------------|
| | | | | | Variant – odd | Variant – even | Variant – odd | Variant – even |
| <i>C432</i> | 550 | 10 | 40 | 550 | M | T | M | T |
| <i>C499</i> | 2200 | 10 | 70 | 2200 | M | T | M | T |
| <i>C1355</i> | 2000 | 10 | 50 | 2000 | M | T | M | T |
| <i>C880</i> | 10000 | 10 | 600 | 10000 | M | T | M | T |
| <i>C1908</i> | 7500 | 15 | 400 | 7500 | M | T | M | T |
| <i>C3540</i> | 16000 | 30 | 400 | 16000 | T | M | T | M |
| <i>S1196</i> | 30000 | 20 | 1500 | 30000 | T | M | T | M |
| <i>S1269</i> | 1000 | 10 | 70 | 1000 | T | M | T | M |
| <i>S1423</i> | 30000 | 12 | 2500 | 30000 | T | M | T | M |
| <i>S832</i> | 18000 | 20 | 700 | 18000 | T | M | T | M |

T – number of pseudo-random test patterns (test length). M – number of deterministic patterns(memory vectors).

5. Results:

| Circuit: | Type I LFSR | | Type II LFSR | |
|----------|-------------|----------------|--------------|----------------|
| | Test Length | Fault Coverage | Test Length | Fault Coverage |
| | | | | |
| | | | | |

Circuit 1: _____

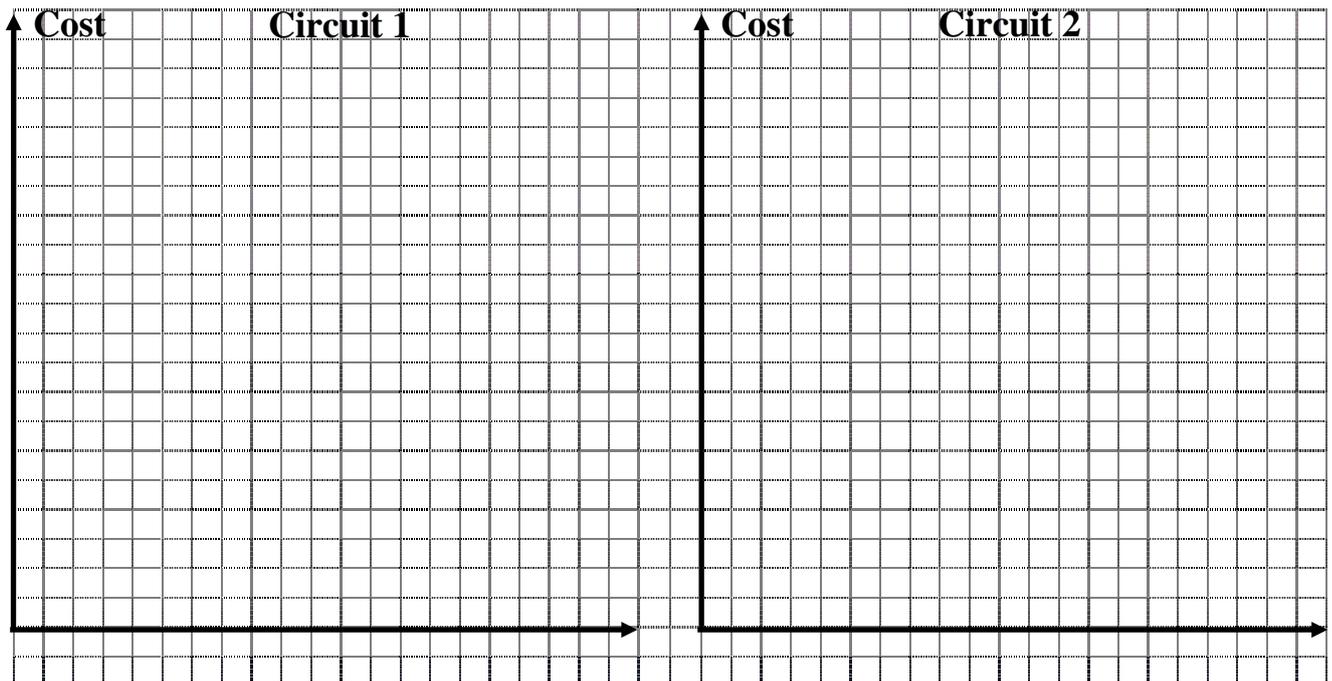
| Reseeding | | | | Hybrid BIST | | | |
|------------------|-------------|----------------|----------------|-----------------|-------------|----------------|----------------|
| Calculated Cost: | Test Length | Memory Vectors | Fault Coverage | Calculated Cost | Test Length | Memory Vectors | Fault Coverage |
| 1. | | | | 1. | | | |
| 2. | | | | 2. | | | |
| 3. | | | | 3. | | | |
| 4. | | | | 4. | | | |
| 5. | | | | 5. | | | |

Circuit 2: _____

| Reseeding | | | | Hybrid BIST | | | |
|------------------|-------------|----------------|----------------|-----------------|-------------|----------------|----------------|
| Calculated Cost: | Test Length | Memory Vectors | Fault Coverage | Calculated Cost | Test Length | Memory Vectors | Fault Coverage |
| 1. | | | | 1. | | | |
| 2. | | | | 2. | | | |
| 3. | | | | 3. | | | |
| 4. | | | | 4. | | | |
| 5. | | | | 5. | | | |

Test Length – number of pseudo-random test patterns. Memory Vectors – number of deterministic patterns.

Present BIST Cost curves on the plot below:



X-axis – Test Length or Memory Vectors (according to your variant)