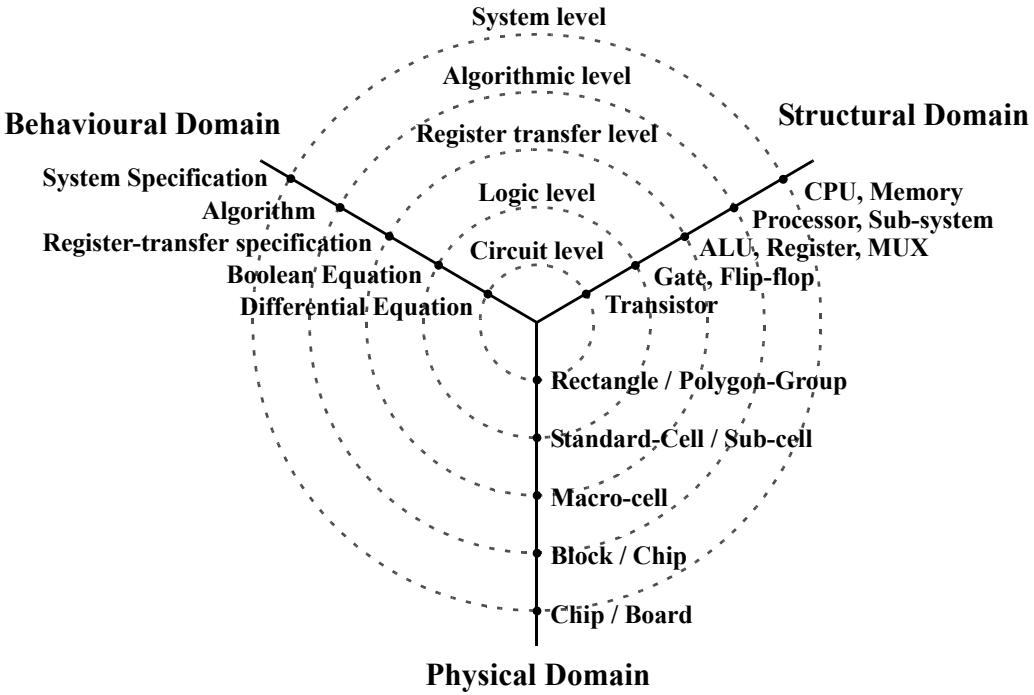
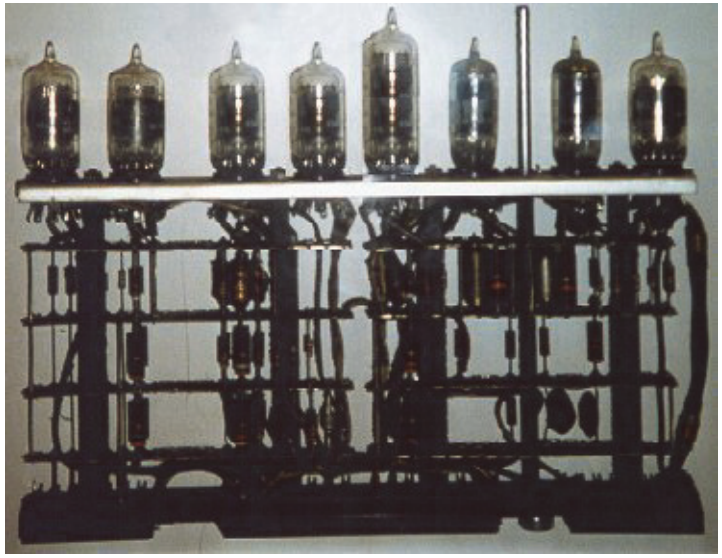
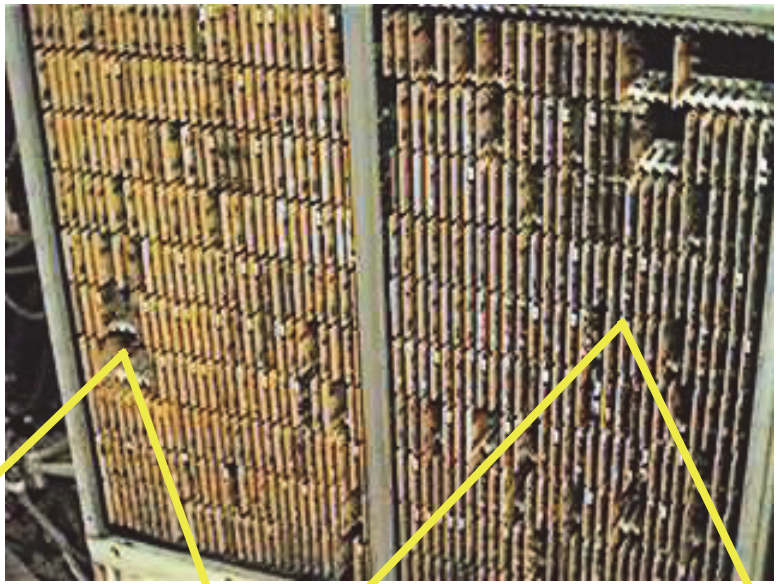
Synthesis at different abstraction levels

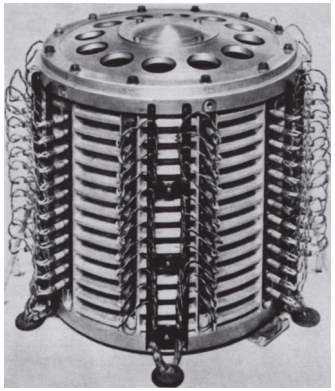
- System Level Synthesis
  - Clustering.
    Communication synthesis.
- High-Level Synthesis
  - Resource or
    time constrained scheduling
  - Resource allocation. Binding
- Register-Transfer Level Synthesis
  - Data-path synthesis.
    Controller synthesis
- Logic Level Synthesis
  - Logic minimization.
    Optimization, overhead removal
- Physical Level Synthesis
  - Library mapping.
    Placement. Routing

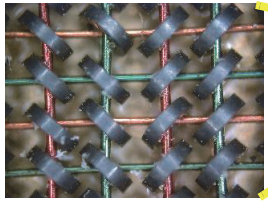


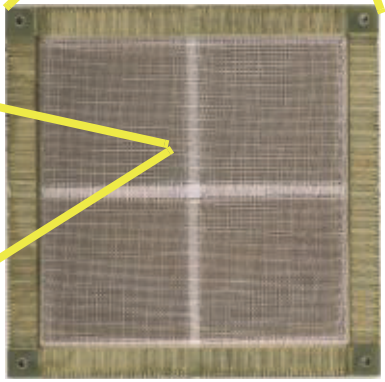
Physical implementation – history

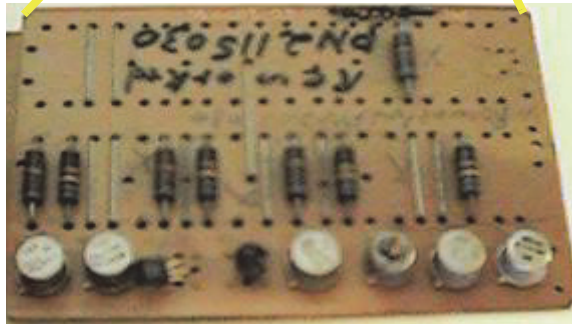




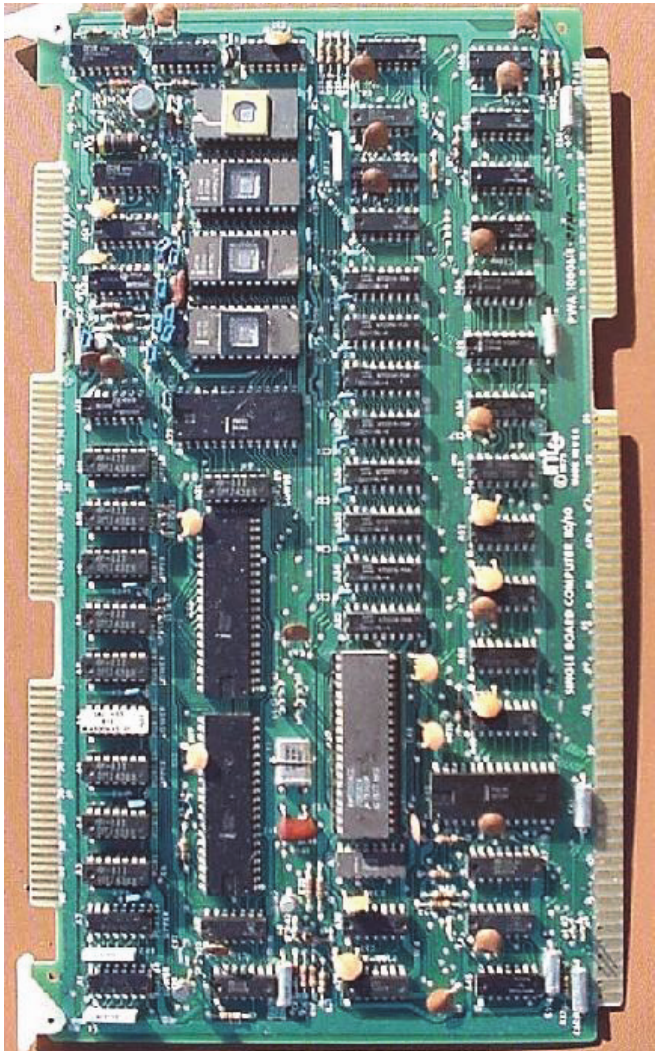


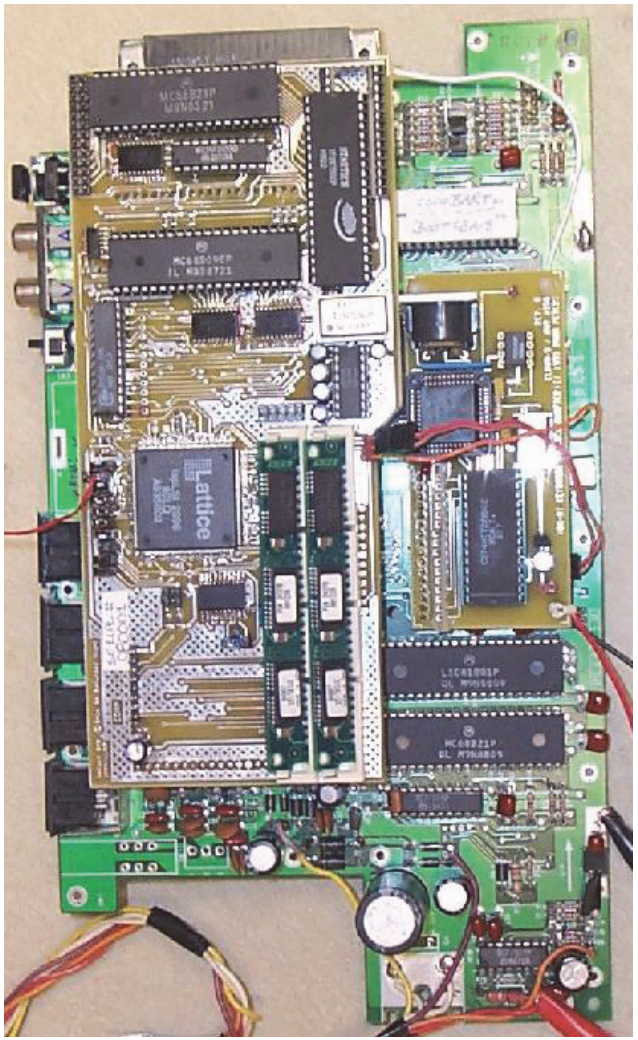


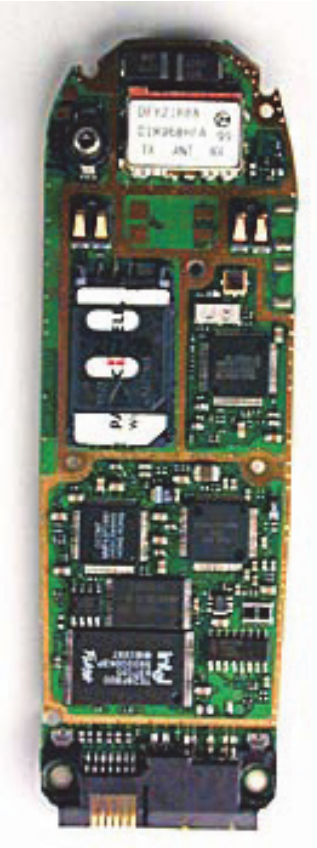




Physical implementation – history

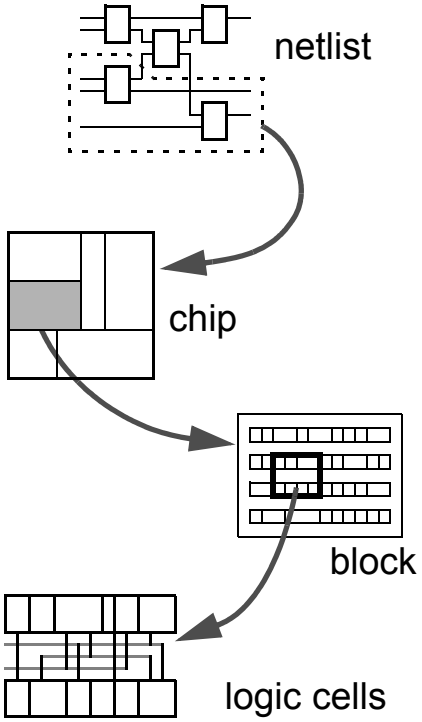


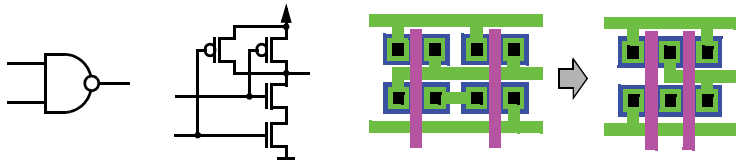




Chip design and fabrication

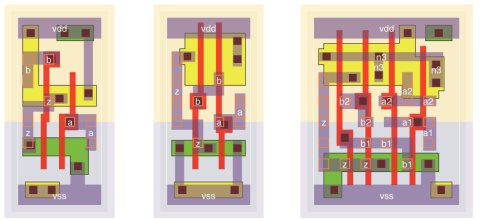
- Partitioning
- Floorplanning
  - initial placement
- Placement
  - fixed modules
- Global routing
- Detailed routing
- Layout optimization
- Layout verification



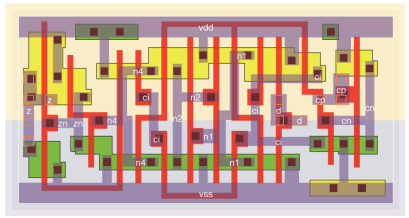


Standard cell examples

2-NAND 2-NOR 2-2-AND-NOR



flip-flop

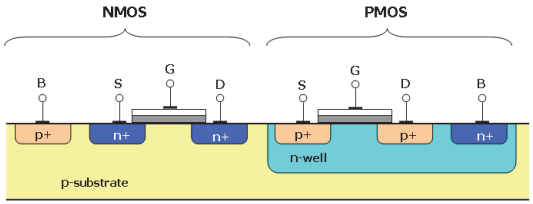


http://www.vlsitechnology.org/

- Fabrication – http://jas.eng.buffalo.edu/ [e.g., 7.2]

CMOS chip fabrication

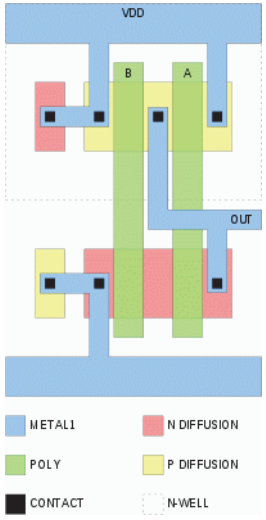
CMOS transistors



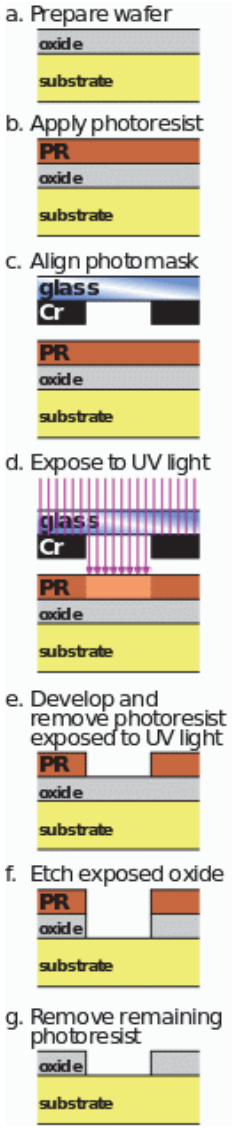
n - electrons [P, As, Sb]

p - holes [B, Al]

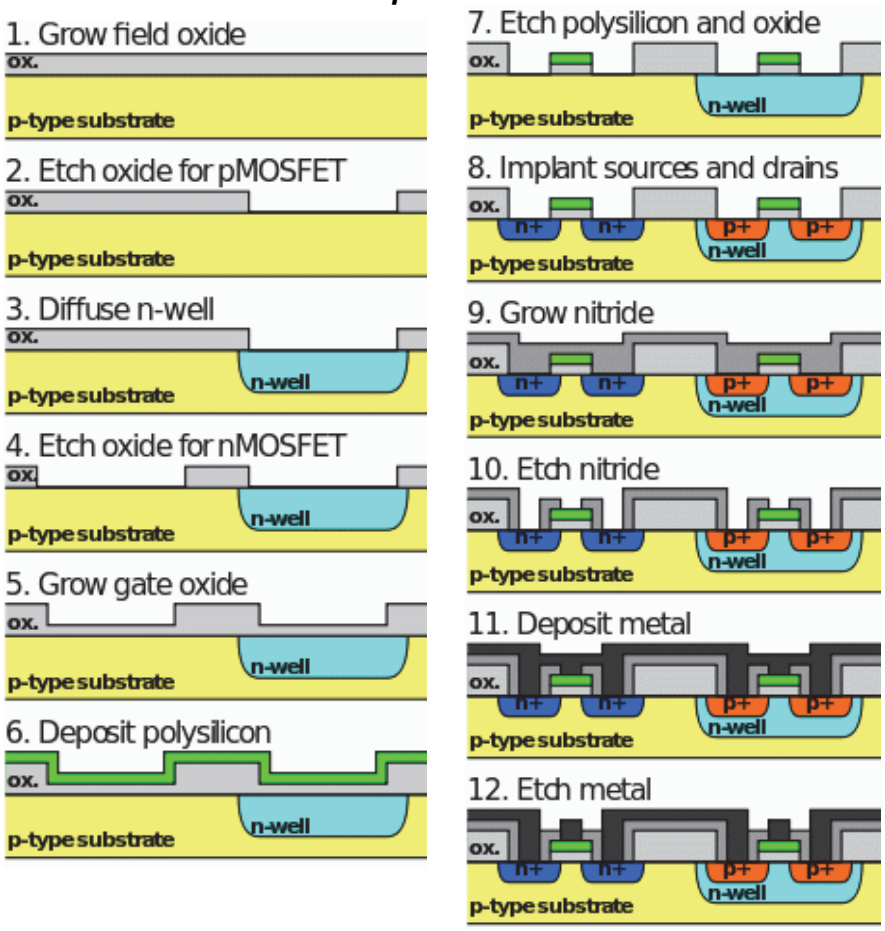
2-NAND layout



etching steps



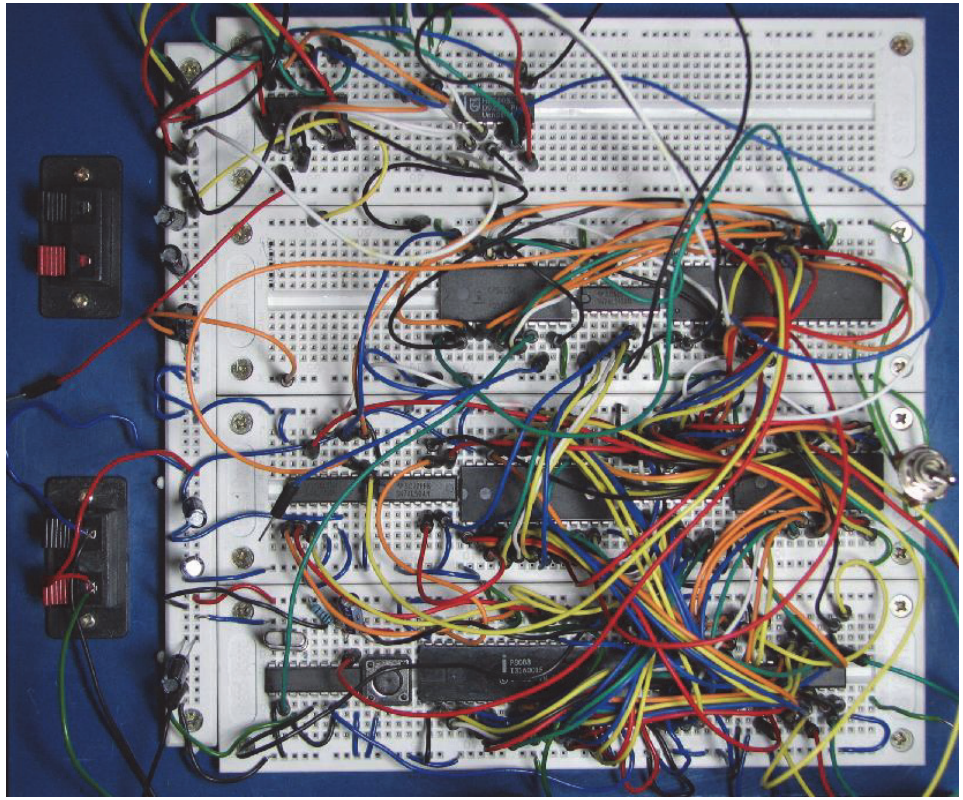
fabrication steps



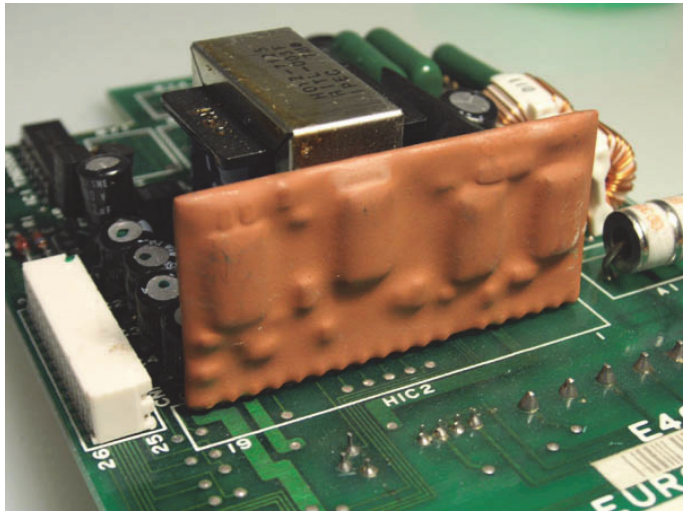
www.wikipedia.org

Packaging examples

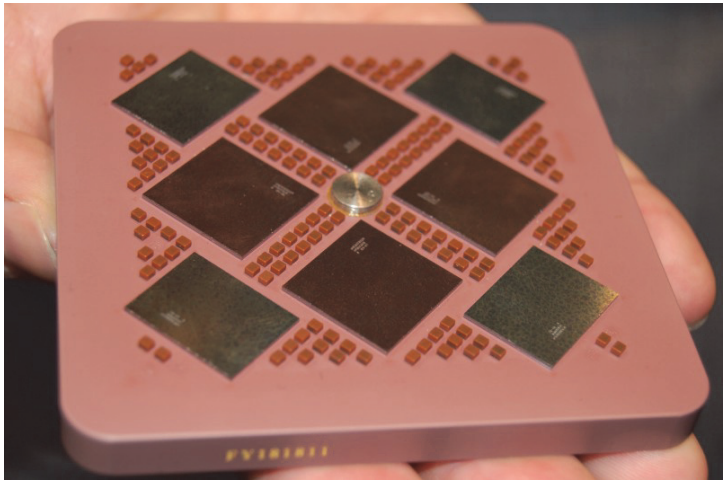
prototyping



hybrid circuit



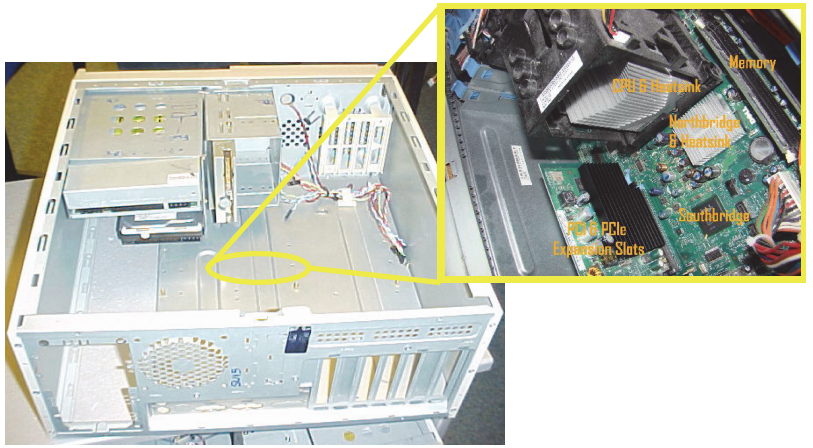
3D assembly

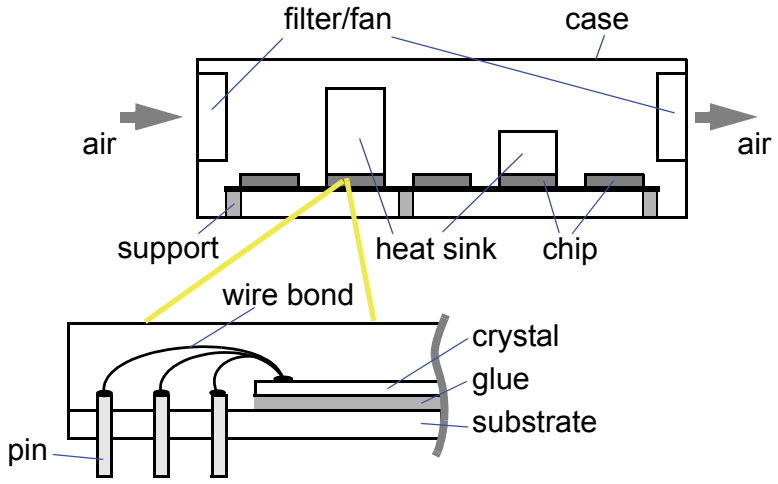


IBM POWER5

Packaging issues

- Mechanical requirements and constraints
  - size, interfaces
  - durability – dust, vibration
- Thermal requirements and constraints
  - work temperature range
  - cooling / heating
- Electrical requirements and constraints
  - power supply
  - protection – voltage, electromagnetic fields
- Ergonomic requirements and constraints
  - appearance, user interface, noise



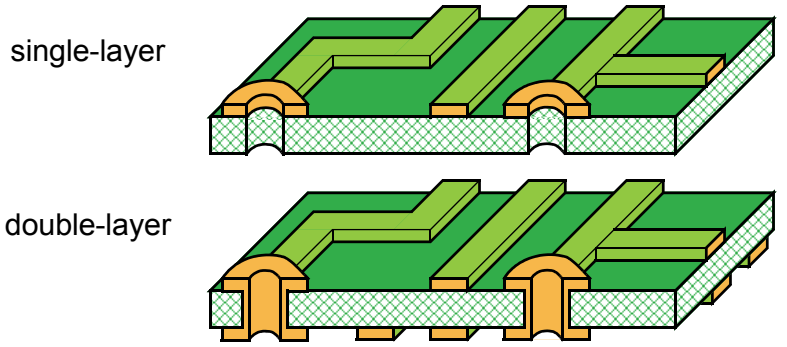


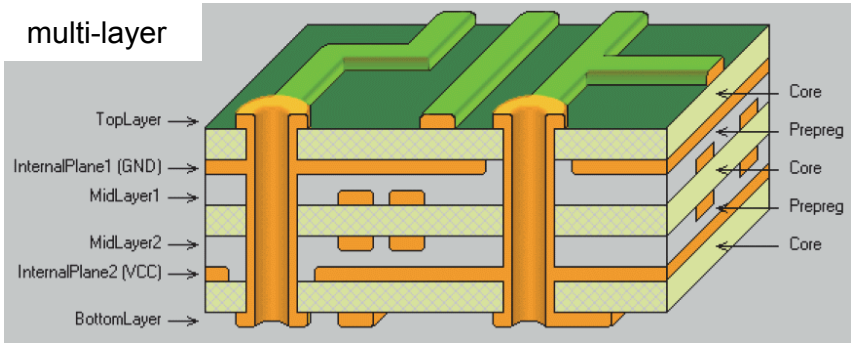
Printed Circuit Board (PCB)

- Components
  - chips, transistors, resistors, capacitors, etc.
- Connections / interfaces / mounting

- PCB manufacturing
- Component placement (and fixing)
- Electrical connections (e.g. soldering)

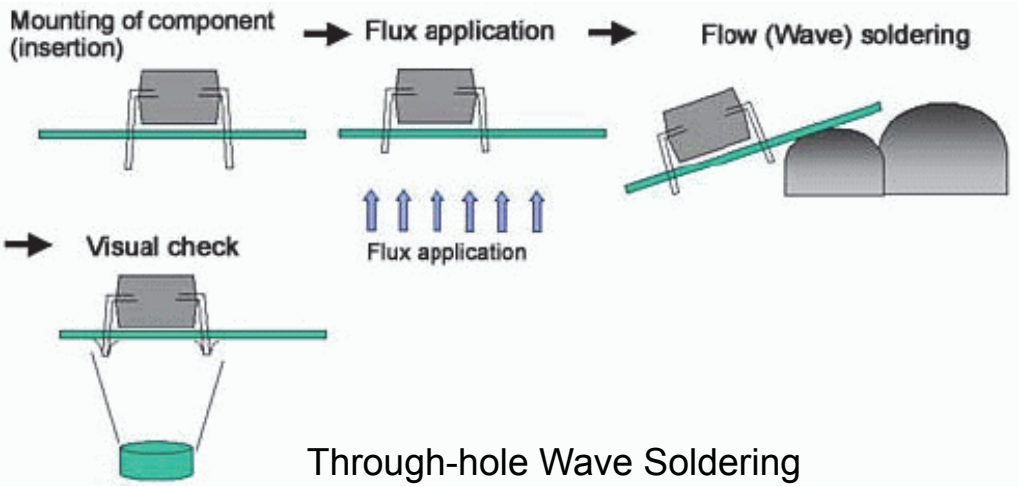
- Single-layer PCB
  - wires (bottom side)
- Double-layer PCB
  - wires + metallized vias
- Multi-layer PCB
  - multiple double-layer PCB-s
  - location of vias!



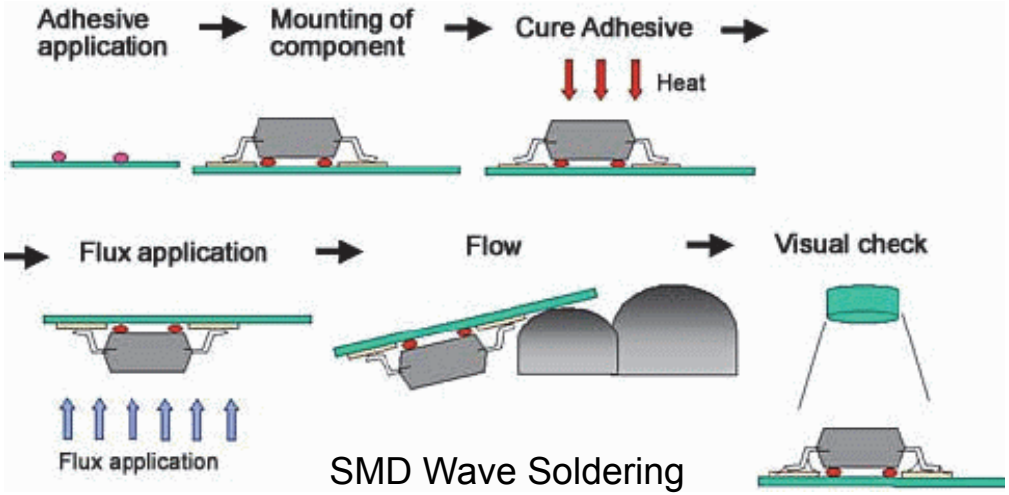


PCB manufacturing

- Manufacturing
  - component mounting
  - soldering
    - solder paste / tin
  - thermal problems
    - large copper surfaces
    - component over-heating
  - quality check
    - visual inspection
  - final finish
    - cleaning
    - protective lacquering
  - final test
    - functional test



Through-hole Wave Soldering



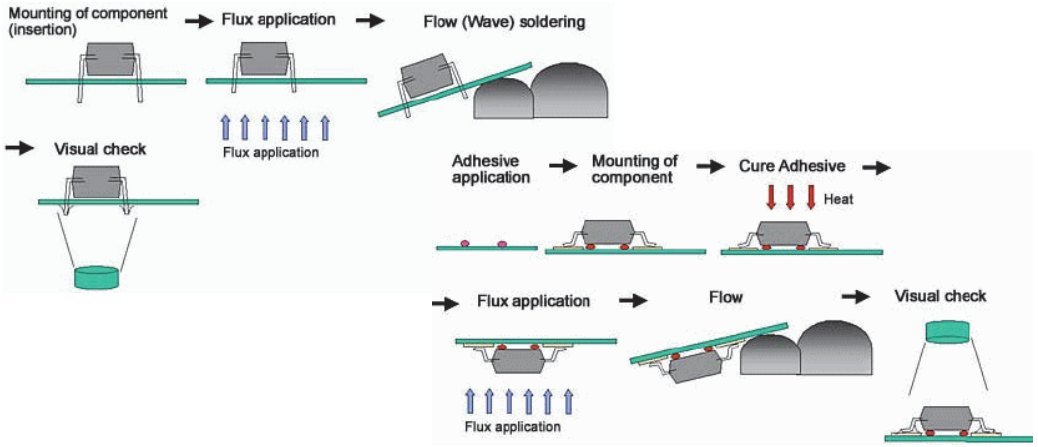
SMD Wave Soldering

PCB manufacturing

Wave Soldering

Electro Soft Inc.
https://www.youtube.com/watch?v=inHzaJIE7-4

Agrowtek Inc.
https://www.youtube.com/watch?v=VWH58QrprVc

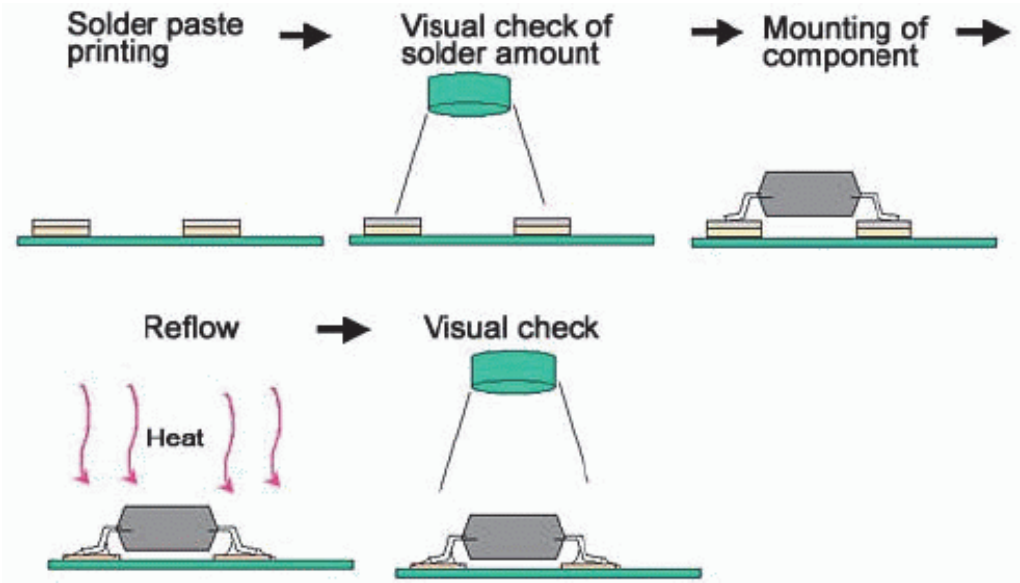


SMD Reflow Soldering

GIGABYTE factory tour
https://www.youtube.com/watch?v=Va3Bfjn4inA

Tutorial
https://www.youtube.com/watch?v=gu0v8lfLcKg

SMD reflow at home
https://www.youtube.com/watch?v=U48Nose31d4



Logic synthesis

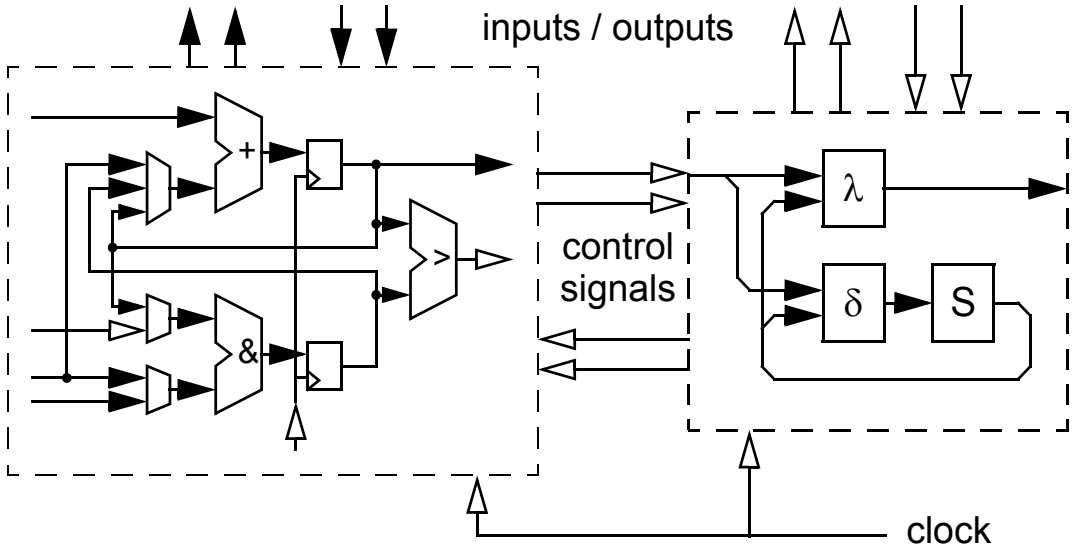
- Transforming logic functions (Boolean functions) into a set of logic gates
  - transformations at logic level from behavioral to structural domain
- Optimizations / Transformations
  - area
  - delay
  - power consumption
- Implementation of Finite State Machines (FSM)
  - state encoding
  - generating next state and output functions
  - optimization of next state and output functions

Logic synthesis – main tasks

- Optimization of representation of logic functions
  - minimization of two-level representation
  - optimization of binary decision diagrams (BDD)
- Synthesis of multi-level combinational nets (circuits)
  - optimizations for area, delay, power consumption, and/or testability
- Optimization of state machines
  - state minimization, encoding
- Synthesis of multi-level sequential nets (circuits)
  - optimizations for area, delay, power consumption, and/or testability
- Library mapping
  - optimal gate selection

Register-transfer level synthesis

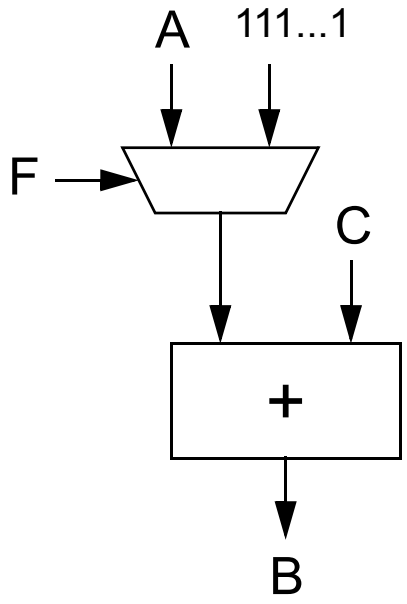
Digital system @RTL = data-path + controller



- *T*ransformation from RT-level structural description to logic level description
- Data-path – storage units (registers, register files, memories) and combinational units (ALU-s, multipliers, shifters, comparators etc.), connected by buses
  - Data path synthesis – maximizing the clock frequency, retiming, operator selection
- Controller – Finite State Machine (FSM) – state register and two combinational units (next state and output functions)
  - Controller synthesis – architecture selection, FSM optimizations, state encoding, decomposition

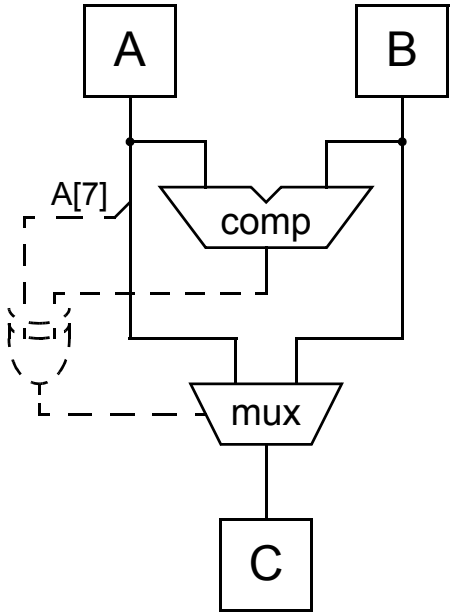
Data-path optimization

```
if F=0 then B := A + C
       else B := C - 1;
```



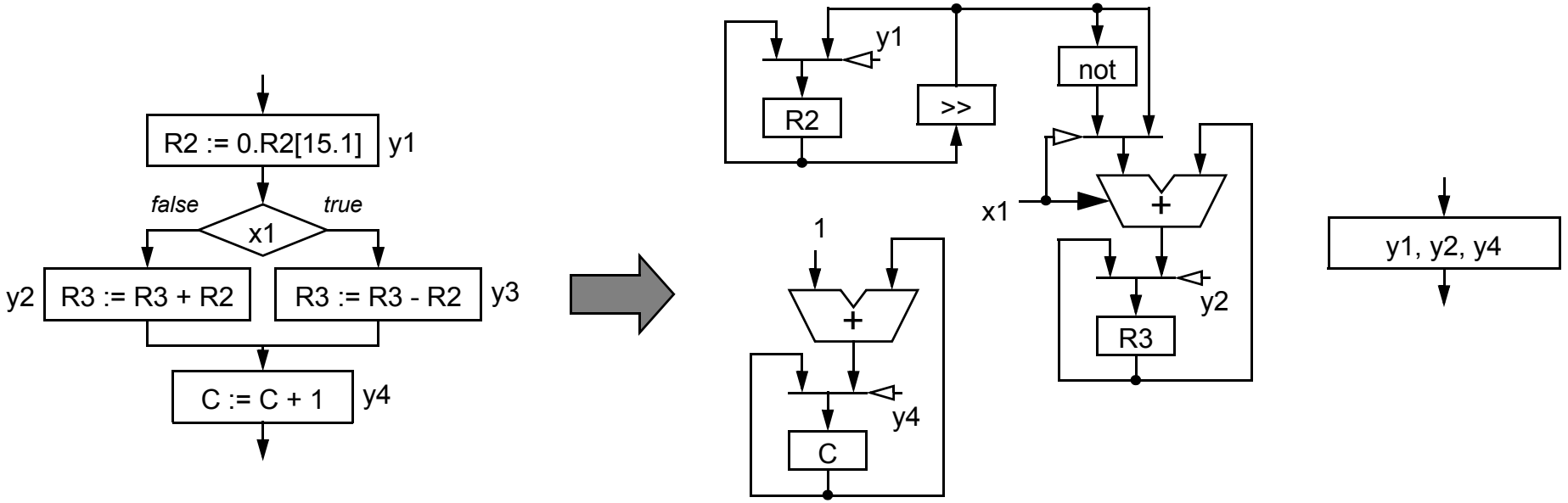

```
read_port(A);
read_port(B);
if A(7)='0' then
  if A>B then
    C := A;
  else
    C := B;
  end if;
else
  if A>B then
    C := B;
  else
    C := A;
  end if;
end if;
```

data flow only
(w/o controller)



Data-path optimization

- **Hardware cost of an operation**
  - **shifting == rerouting wires**
  - **the same functional unit for addition and subtraction – adder (+carry)**
- **Independent operations can be executed simultaneously**
  - **analysis of real data dependencies, e.g., result of shifting R2**



Arithmetic unit architecture selection

- Parallel versus sequential execution
- Adder/subtracter architectures
  - ripple-carry – sequence of full-adders, small but slow
  - carry-look-ahead – separate calculation of carry generation and/or propagation
    - generation: $g_i=a_i \cdot b_i$; propagation: $p_i=a_i+b_i$; carry: $c_i=g_i+p_i \cdot c_{i-1}$
  - carry-select adders – duplicated hardware plus selectors
    - speculative calculation one case with carry and another without, the answer will be selected when the actual carry has arrived
- Multiplier architectures
  - sequential algorithms – register + adder, 1/2/... bit(s) at a time
  - “parallel” algorithms – array multipliers – AND gates + full-adders
- Multiplication/division with constant
  - shift+add – 5*n = 4*n + n = (n<<2) + n

http://www.ecs.umass.edu/ece/koren/arith/simulator

Carry Look Ahead Adder With Timing

Carry Look Ahead Adder

A: 00101110
B: 01100010
bin ◉ *dec* ○

Total Bits 8 Group Size 4

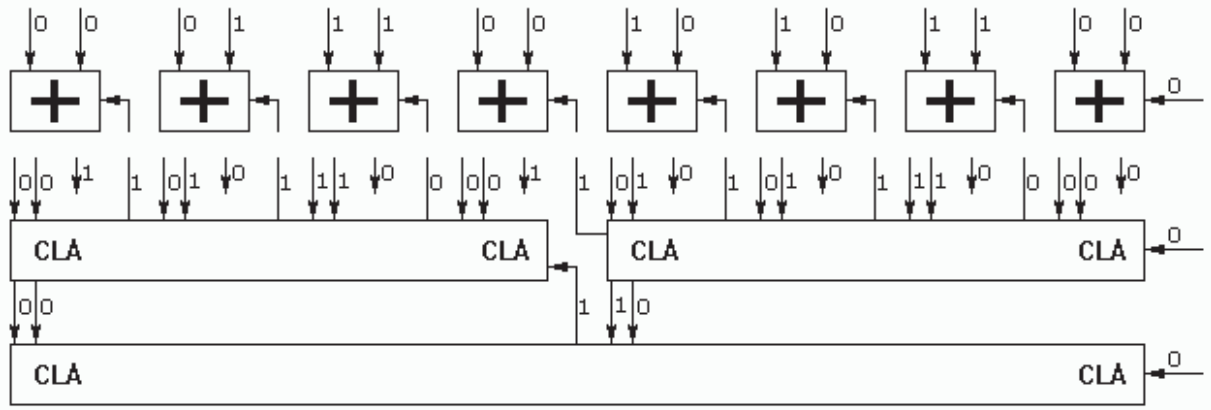
Signal Delays

AND/OR Gate Delay	1.0
XOR Gate Delay	1.6
Maximum Fan-in	4

Compute

Reset

Help



A 00101110 :46
B +01100010 :98

Sum 10010000 :**144**

Time taken to generate all Sum bits - (10.2)units

Delays to calculate Sum in each bit position

BitNumber	7	6	5	4	3	2	1	0
SumDelay	(10.2)units	(10.2)units	(10.2)units	(10.2)units	(7.2)units	(7.2)units	(7.2)units	(7.2)units

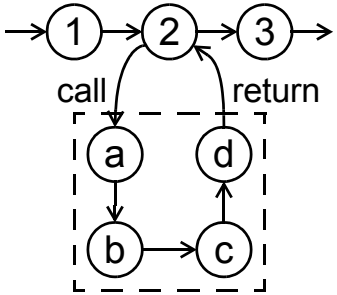
Controller synthesis

- Controller == Finite State Machine (FSM)
- Controller synthesis is also a task at the algorithmic level. Controller is the implementation of the operation scheduling task in hardware.
- *The canonical implementation* of a sequential system is based directly on its state description. It consists of *state register*, and a *combinational network* to implement the transition and output functions.
- Sub-tasks
  - generation of the state graph
  - selecting the proper controller architecture
  - finite state machine optimization for area, performance, testability, etc.

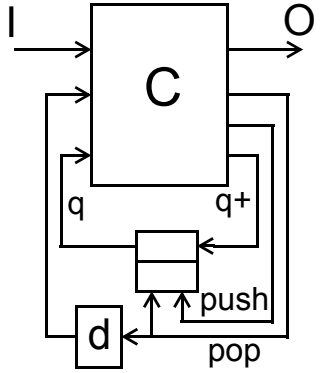
FSM encoding

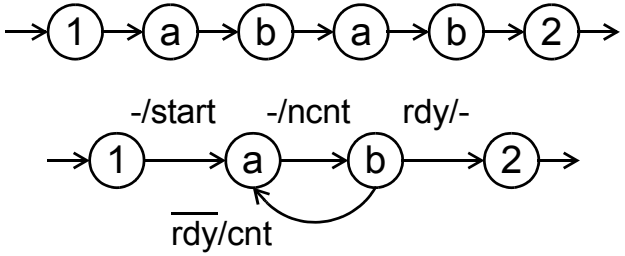
- Input/output encoding – symbols –> binary code
- State encoding – states –> binary code
- *z* – number of symbols/states –> minimum code length is t=ceil($\log_2 z$)
- Two border cases – minimal code length encoding & one-hot-encoding
- General encoding strategy
  - Identification of sets of states (adjacent groups) in the state table such that, if encoded with the minimal Hamming distance, lead to a simplification of the corresponding next-state and output equations after logic minimization.
  - The groups and their intersections are analyzed with the respect of the degree of potential minimizations during the subsequent logic minimization. Results are reflecting the potential gains in the cost of the final logic.
  - Coding constraints and calculated gains control the encoding heuristics which try to satisfy as much constraints as possible.

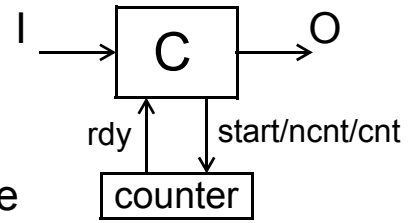
FSM architectures



Stack architecture

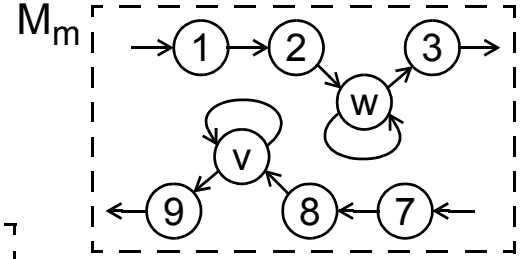


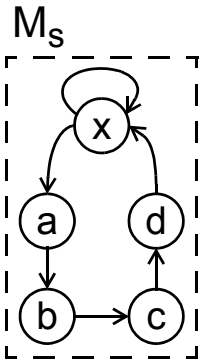


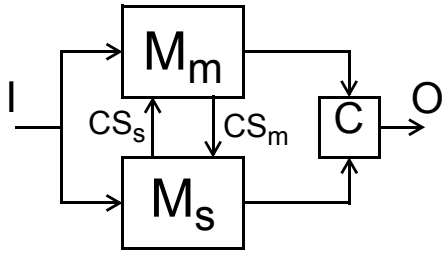


Counter architecture

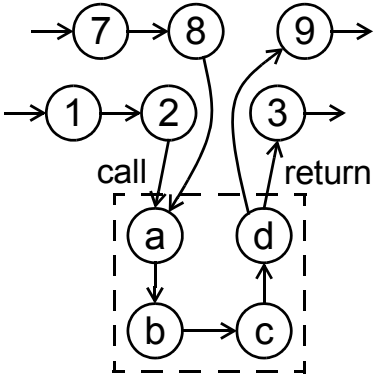
Decomposed architecture

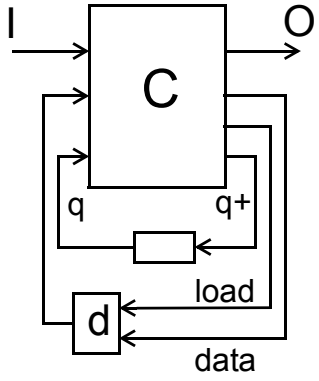






Register architecture





High-Level Synthesis

a.k.a. Behavioral Synthesis a.k.a. Algorithm Level Synthesis

a.k.a. Silicon Compilation

- *High-Level Synthesis* (HLS) takes a specification of the functionality of a digital system and a set of constraints, finds a structure that implements the intended behavior, and satisfies constraints
- Front-end tasks:
  - Mapping PL/HDL decription inot internal graph-based representation
  - Compiler optimizations
- Back-end tasks:
  - Behavioral transformations
  - Essential subtasks – transforming data and control flow into RT level structure
    - scheduling – time or resource constrained
    - resource allocation – functional units, storage elements, interconnects
    - resource assignment (binding) – functional units, storage elements, interconnects
  - Netlist extraction, state machine table generation

Target

- SW synthesis (compilation)
  - input – high-level programming language
  - output – sequence of operations (assembler code)
- HW synthesis (HLS)
  - input – hardware description language
  - output – sequence of operations (microprogram)
  - output – RTL description of a digital synchronous system (i.e., processor)
    - data part & control part
    - communication via flags and control signals
    - discrete time steps (for non-pipelined designs *time step* = *control step*)
- Creating the RTL structure means mapping the data and control flow in two dimensions – time and area

Scheduling

- Scheduling – assignment of operations to time (control steps), possibly within given constraints and minimizing a cost function
  - transformational and constructive algorithms
  - use potential parallelism, alternation and loops
  - many good algorithms exist, well understood
- Resource constrained scheduling (RCS)
  - List scheduling
- Time constrained scheduling (TCS)
  - ASAP – “as soon as possible” / ALAP – “as late as possible”
  - ASAP and ALAP scheduling are used for
  - Force directed scheduling
- Neural net based schedulers
- Path-based / path traversing scheduling (AFAP)

Allocation and binding

- High-level synthesis tasks, i.e., scheduling, resource allocation, and resource assignment neither need to be performed in a certain sequence nor to be considered as independent tasks
- Allocation is the assignment of operations to hardware possibly according to a given schedule, given constraints and minimizing a cost function
- Functional unit, storage and interconnection allocations
  - slightly different flavors:
    - module selection – selecting among several ones
    - binding – to particular hardware (a.k.a. assignment)
- Other HLS tasks...
  - *Memory management*: deals with the allocation of memories, with the assignment of data to memories, and with the generation of address calculation units
  - *High-level data path mapping*: partitions the data part into application specific units and defines their functionality
  - *Encoding* data types and control signals

Completing the Data Path

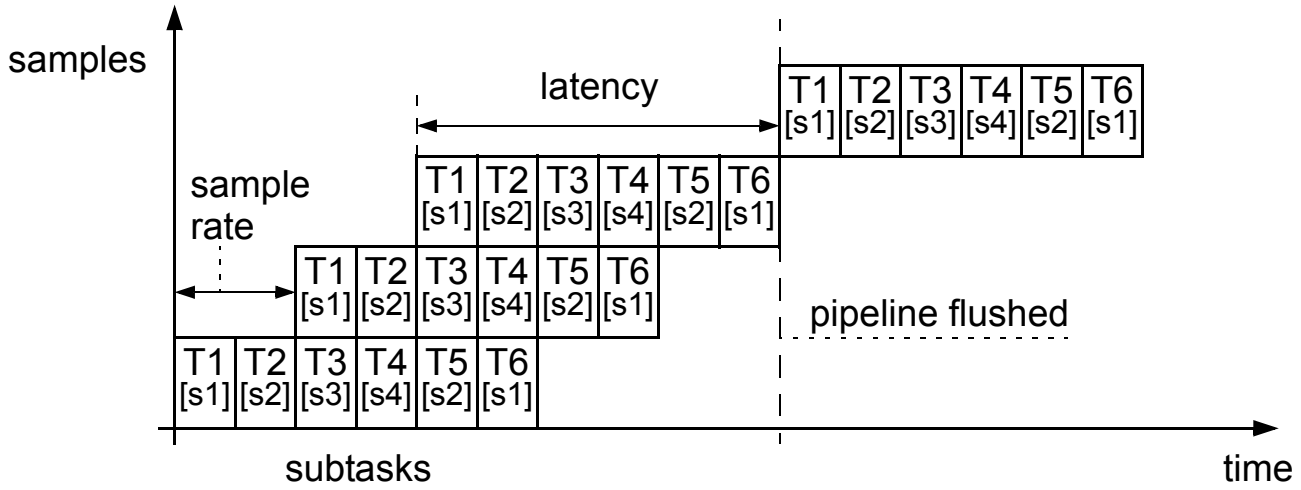
- Subtasks after scheduling
  - Allocation
    - Allocation of FUs (if not allocated before scheduling)
    - Allocation of storage (if not allocated before scheduling)
    - Allocation of busses (if buses are required and not allocated in advance)
  - Binding (assignment)
    - Assignment of operations to FU instances
      (if not assignment before scheduling as in the partitioning approach)
    - Assignment of values to storage elements
    - Assignment of data to be transferred to buses (if busses are used)
- Allocation and binding approaches
  - Rule based schemes (Cathedral II), used before scheduling
  - Greedy (e.g., Adam)
  - Iterative methods
  - Branch and bound (interconnect levels)
  - Integer linear programming (ILP)
  - Graph theoretical (clicks, node coloring)

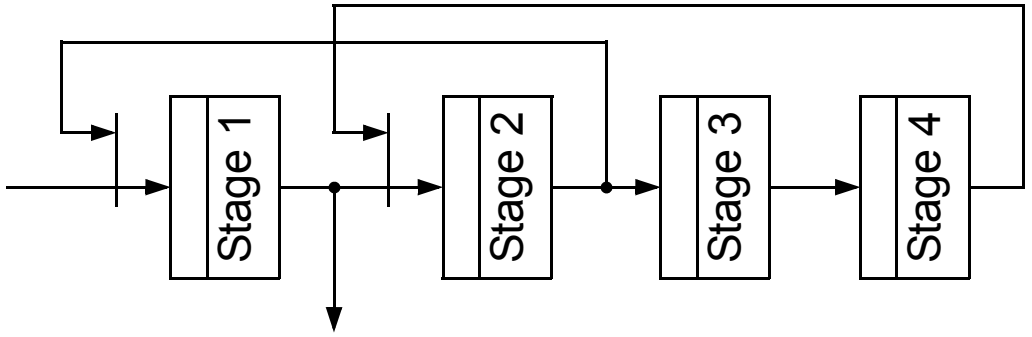
Pipelining

- *Pipelining* - an implementation technique whereby multiple instructions are overlapped in execution
- *Latency (L)* - total number of time units needed to complete the computation on one input sample
- *Sample rate (R)* - the number of time units between two consecutive initiations, where initiation is the start of a computation on an input sample
- *A (pipe) stage* is a piece of HW that is capable of executing certain subtask of the computation
- *The reservation table* is a two-dimensional representation of the data flow during one computation. One dimension corresponds to the stages, and the other dimension corresponds to time units.

- Actions in pipeline: *flushing*, *refilling*, *stalling*.

Pipeline - example





Pipeline measurements

- Average initiation rate (measure of pipeline performance):

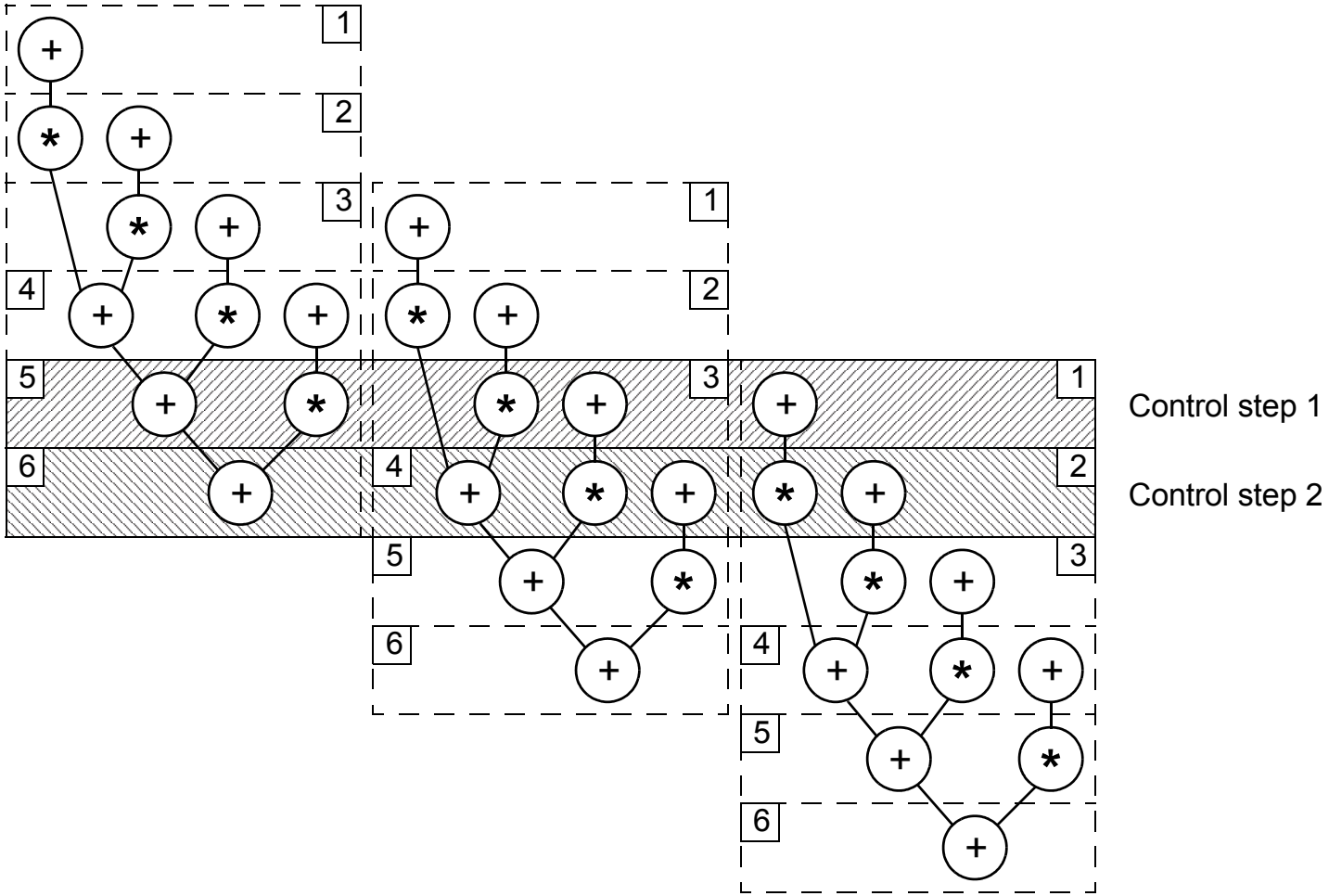
$$R_{init,N\to\infty} = 1 / (R \times t_{stage} + r_{synchro} \times (L-R) \times t_{stage})$$

  - R -sample rate, L - latency,
  - t_{stage} - the time one stage needs to complete its subtask,
  - $r_{synchro} = N_{flush} / N$ - resynchronization rate,
  - N_{flush} - the number of input samples that cause flushing,
  - N - number of input samples.

Functional pipelining

- In conventional pipelining, stages have physical equivalents, i.e. the stage hardware is either shared completely in different time units or not shared at all.
- In the case of large functional units, there is no physical stage corresponding to the logical grouping of operations in a time step.
- A *control step* corresponds to a group of time steps that overlap in time. Operations belonging to different control steps may share functional units without conflict.
- Operations, belonging to the time steps $s+n\times L$, for $n\geq 0$, are executed simultaneously and cannot share hardware.

Functional pipelining of 8-point FIR filter



Retiming

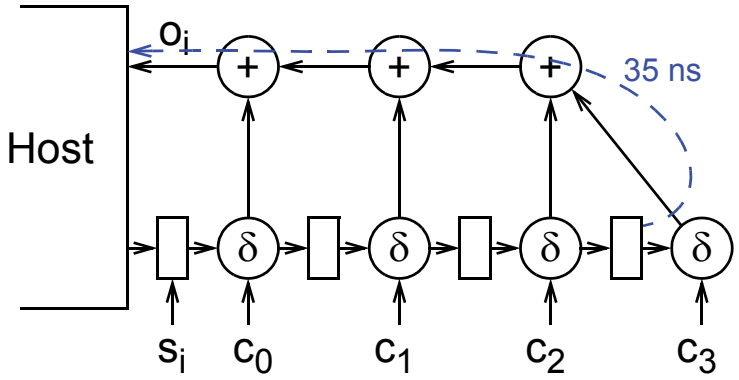
- Minimization of the cycle-time or the area of synchronous circuits by changing the position of the registers
  - cycle-time <- critical path
- The number of registers may increase or decrease
  - area minimization corresponds to minimizing the number of registers
  - combinational circuits are not affected (almost)
- Synchronous logic network
  - variables / boolean equations / synchronous delay annotation

Retiming at higher abstraction levels?

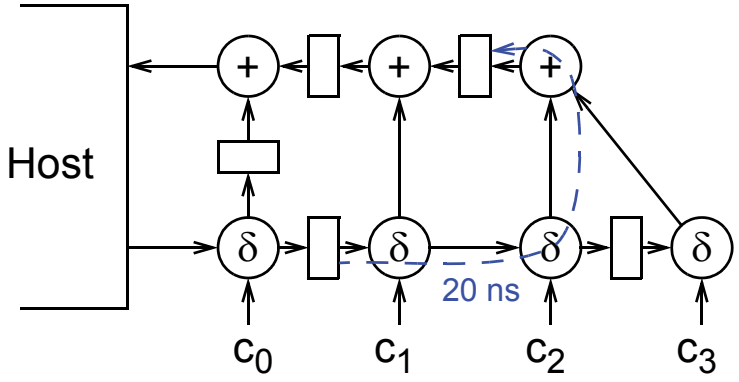
- The same, in principle, as for logic networks
  - operation nodes - functions / delay nodes - e.g. shared resources (memories)
- More possibilities to manipulate the functions - higher complexity of the optimization task
  - partitioning/merging functions
  - reorganizing shared resources

Retiming: example #2

Digital correlator



Before



After

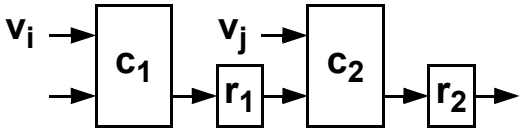
$$o_i = \sum_{j=0}^{3} \delta(s_{i-j}, c_j)$$

+ 10 ns

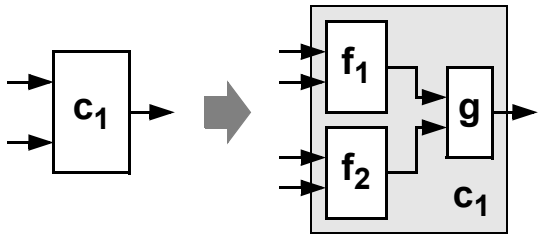
δ 5 ns

Retiming at higher abstraction levels

- **Optimization:**
  - control-step #1: $r_1 \leftarrow c_1(v_i,...)$,
  - control-step #2: $r_2 \leftarrow c_2(r_1,v_j,...)$
  - r_1,r_2 - registers; c_1,c_2 - combinational blocks; v_i,v_j - variables



  - $f_{max} = 1 / \max(delay(c_1),delay(c_2))$,
  - $delay(c_1) > delay(c_2)$: then $c_1^{new} = g(f_1(v_i,...), f_2(v_i,...))$



- **After resynthesis, $delay(g)+delay(c_2) < delay(c_1)$:**
  - control-step #1: $r_1 \leftarrow f_1(v_i,...)$; $r_x \leftarrow f_2(v_i,...)$
  - control-step #2: $r_2 \leftarrow c_2(g(r_1,r_x),v_j,...)$