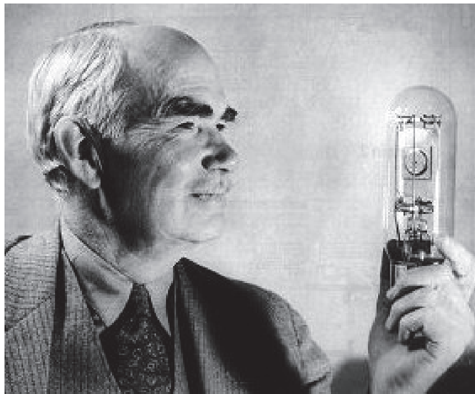
Physical Level Design

IAS0600 Digital Systems Design with VHDL

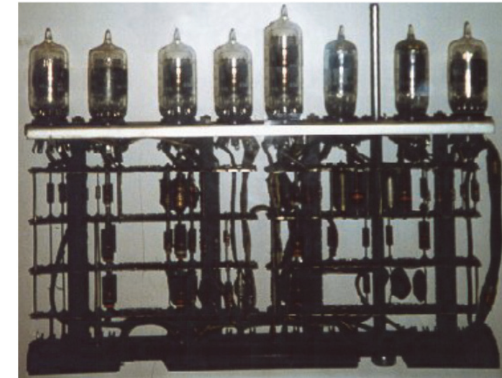
Peeter Ellervee, Jaan Raik

How did we get there?

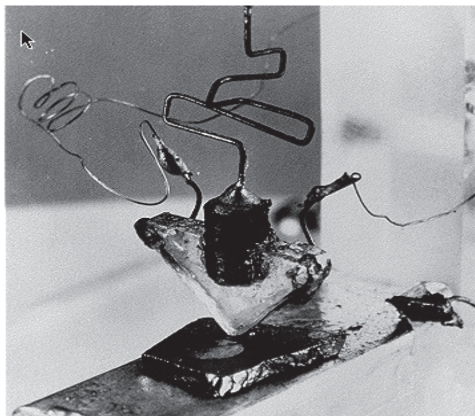
1906



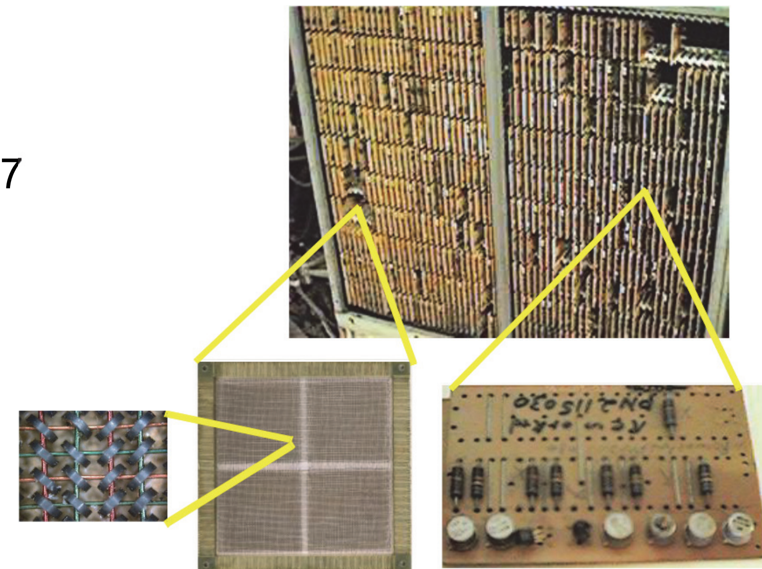
Audion (Triode), 1906
Lee De Forest



1947

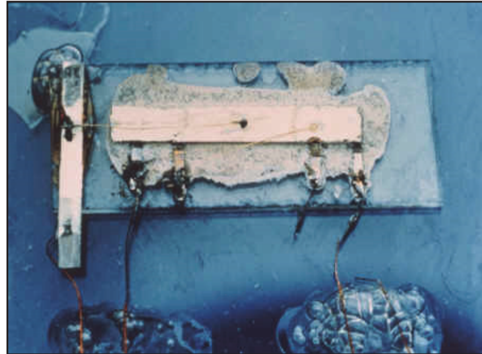


First point contact
transistor (Ge), 1947
John Bardeen and
Walter Brattain
Bell Laboratories

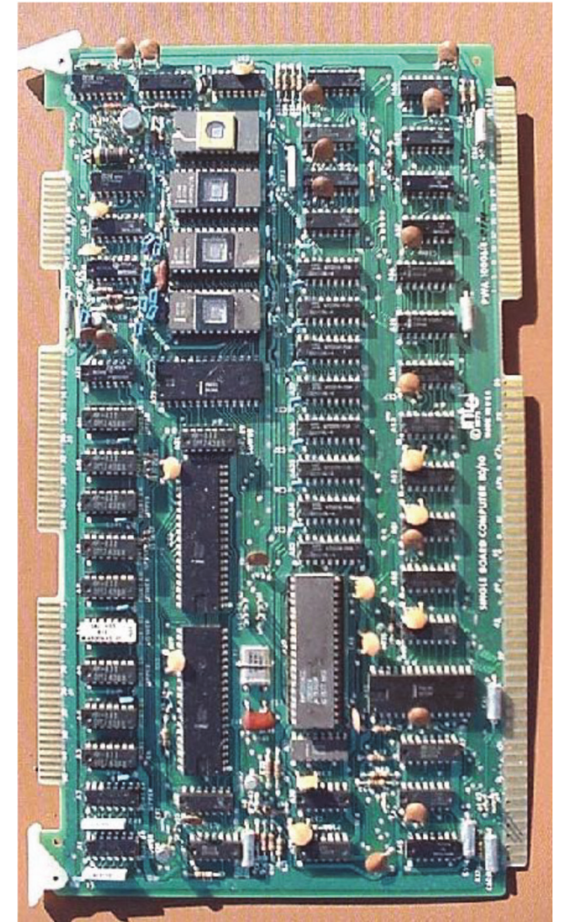


How did we get there?

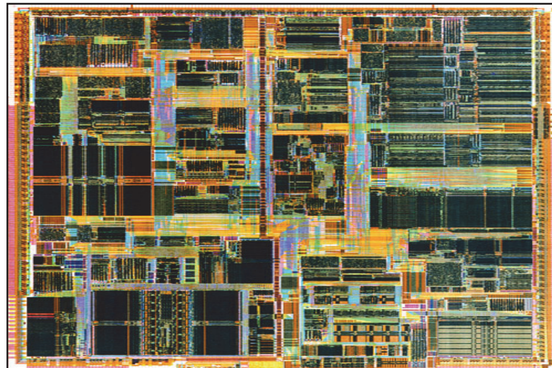
1958



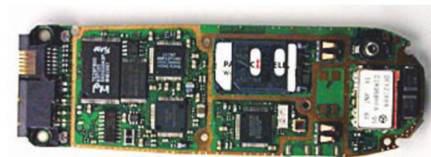
First integrated circuit (Ge), 1958
Jack S. Kilby, Texas Instruments
transistors resistors and capacitors



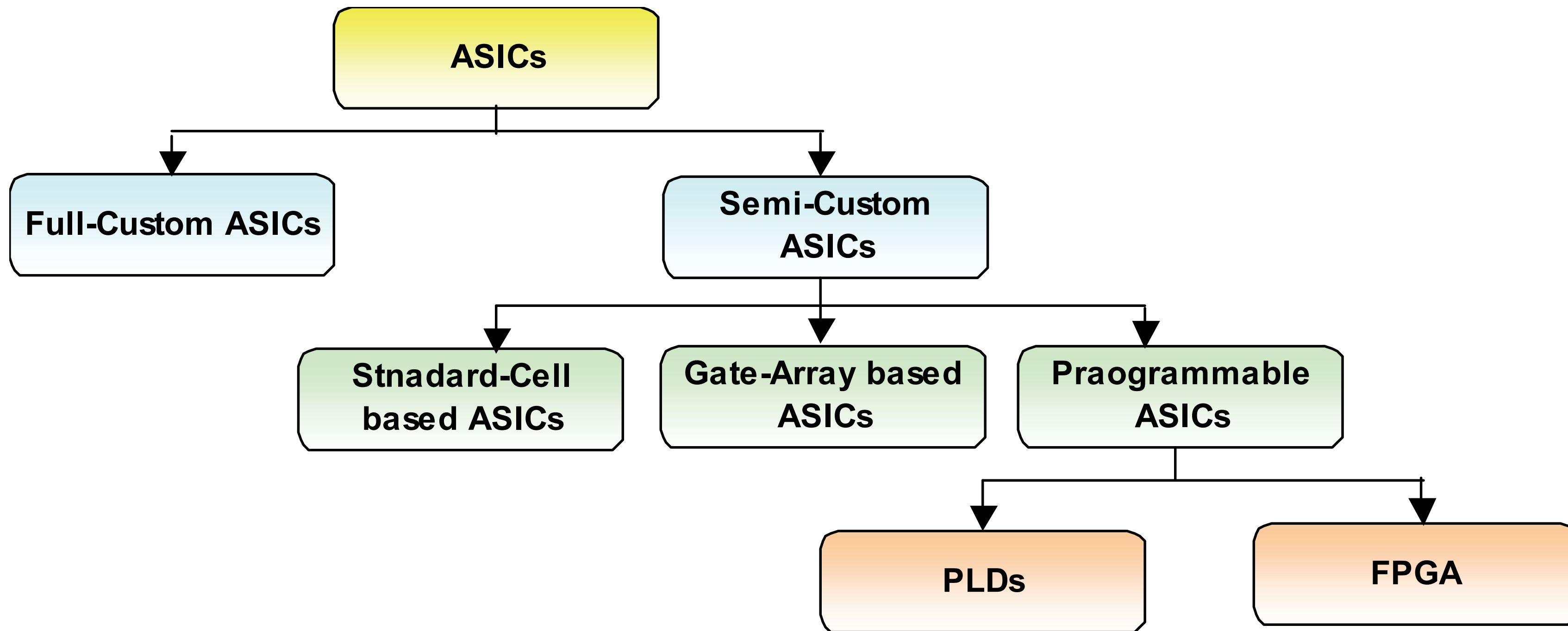
1997



Intel Pentium II, 1997
Gate Length: 0.35, Clock: 233MHz
Number of transistors: 7.5 M



ASIC – Application Specific Integrated Circuit



Full-Custom ASICs: Possibly all logic cells and all mask layers customized

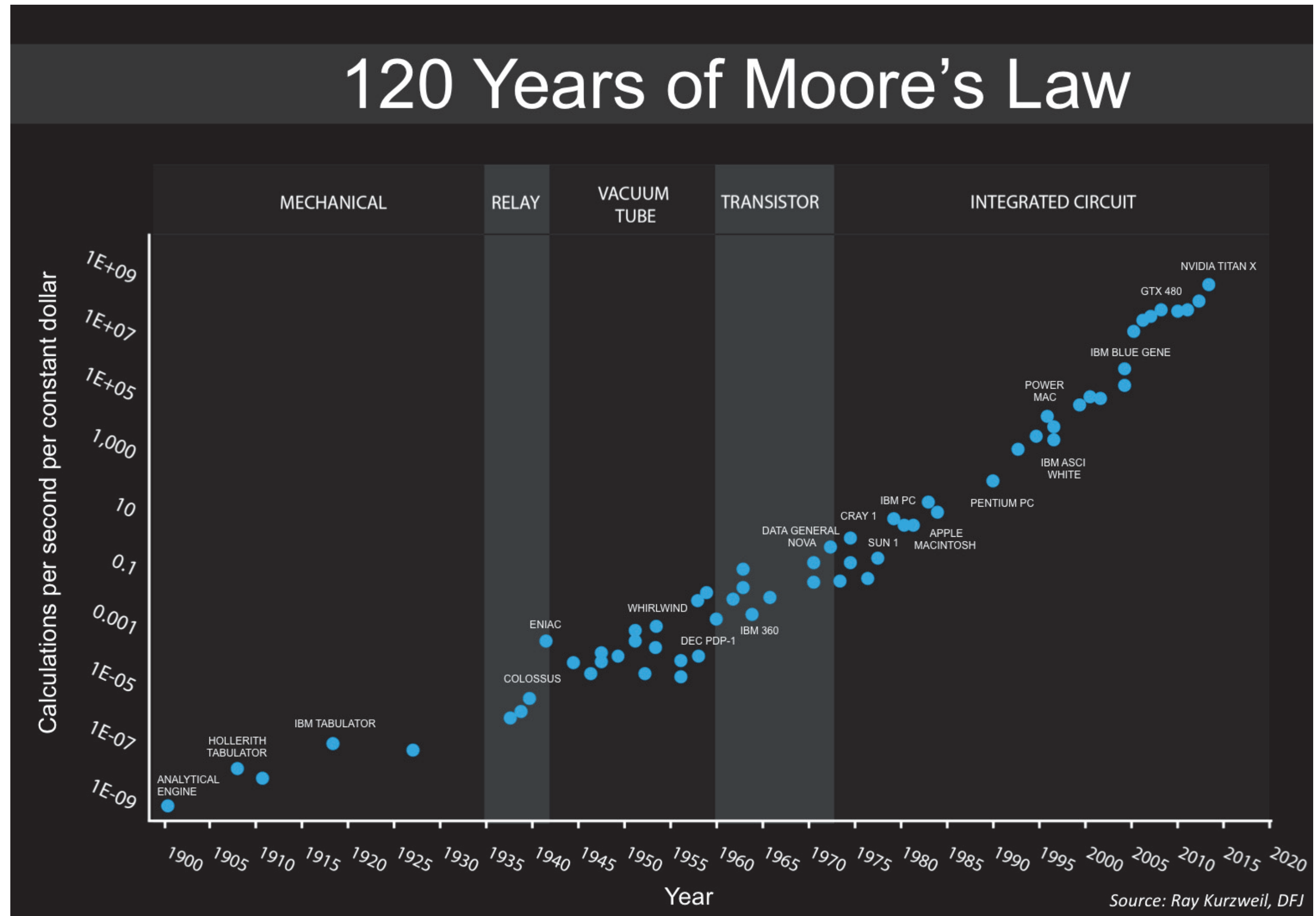
Semi-Custom ASICs: all logic cells are pre-designed and some (possibly all) mask layers customized

Moore's law (1965)

"Essential parameters of digital devices double each 18 months."

Speed & cost of calculations

wikipedia



VLSI/ASIC – physical level design

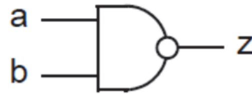
2-NAND

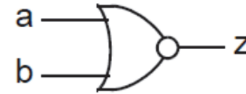
2-NOR

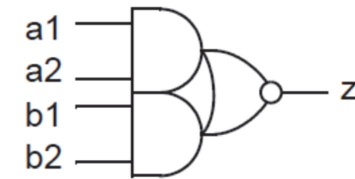
2-2-AND-NOR

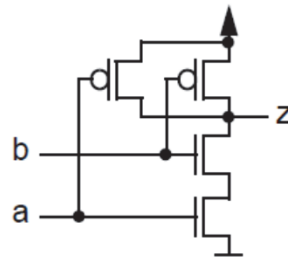
Logic level

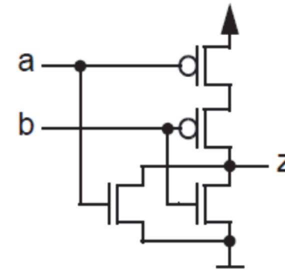
- logic gates / logic expressions
- circuits / bits

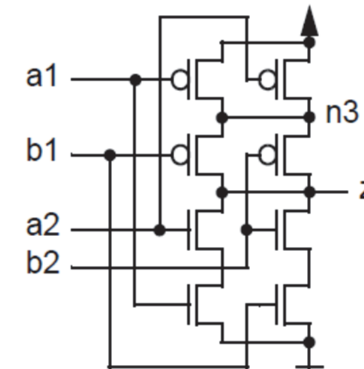






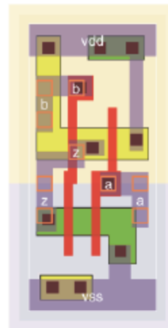


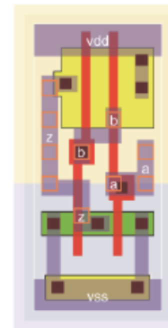


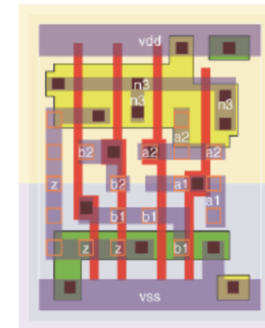


Physical level

- transistors / wires
- polygons





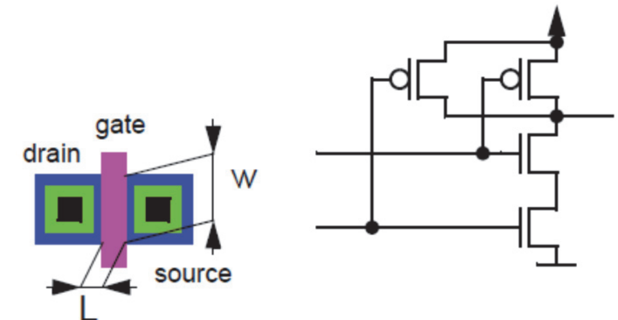


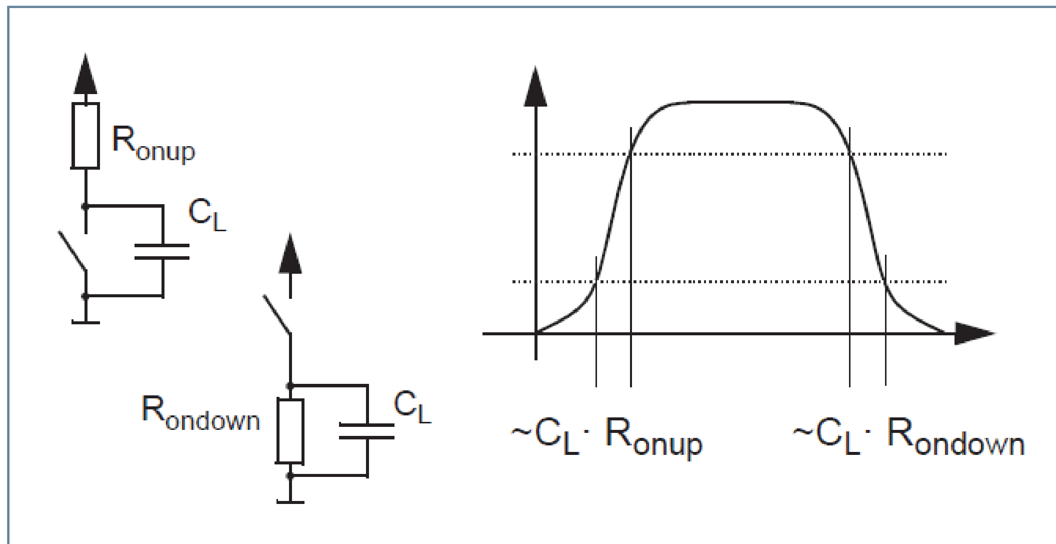
http://www.vlsitechnology.org/

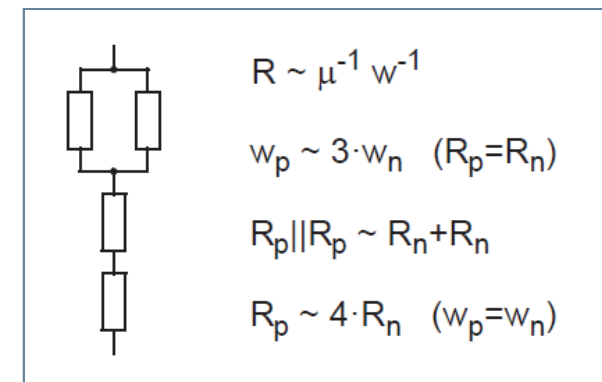
CMOS – why NAND?

Material properties – <u>mobility</u> –
$\mu_n = 1250\ cm^2 / V\ sec$ & $\mu_p = 480\ cm^2 / V\ sec$

$R \sim \mu^{-1}$ & $R \sim L\ w^{-1}$ (L - constant)

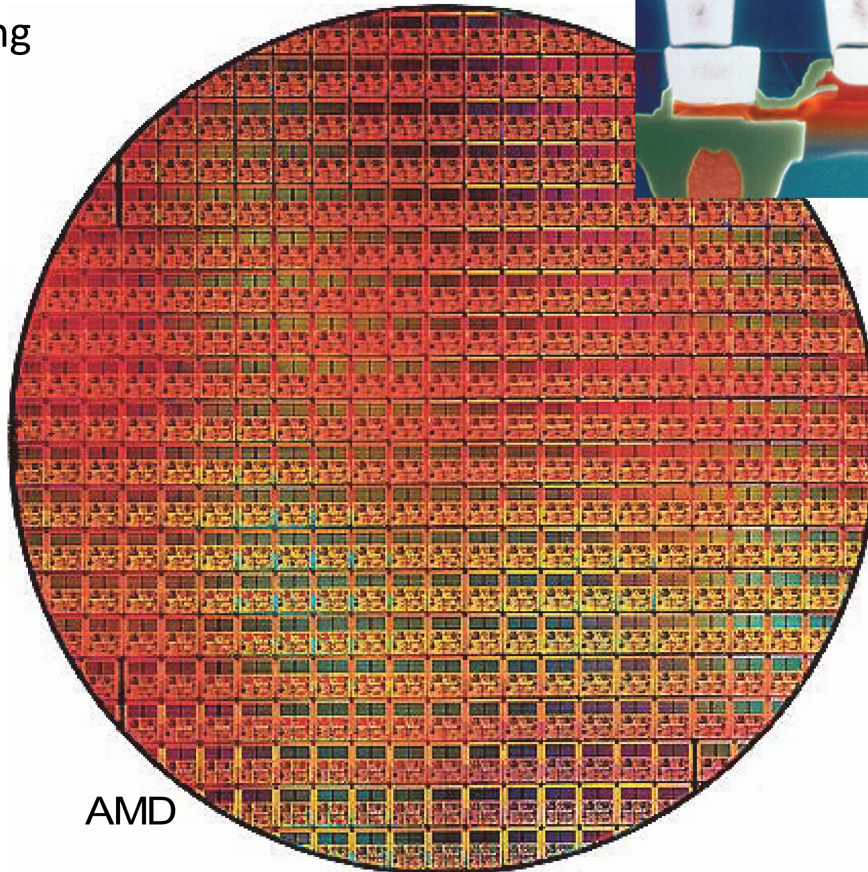




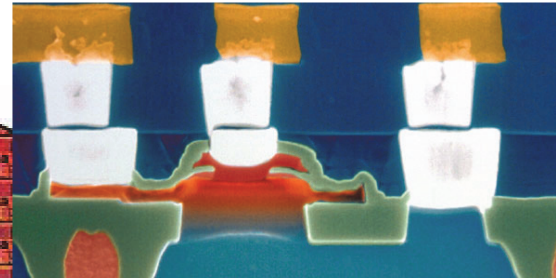


Chip manufacturing

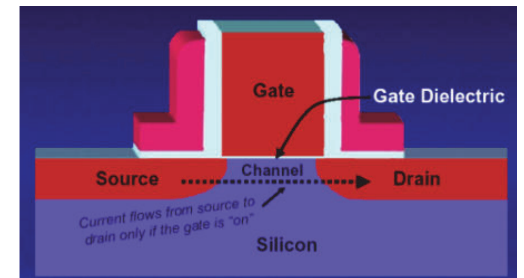
- masks – exposing & developing
- etching / adding
- packaging
- testing

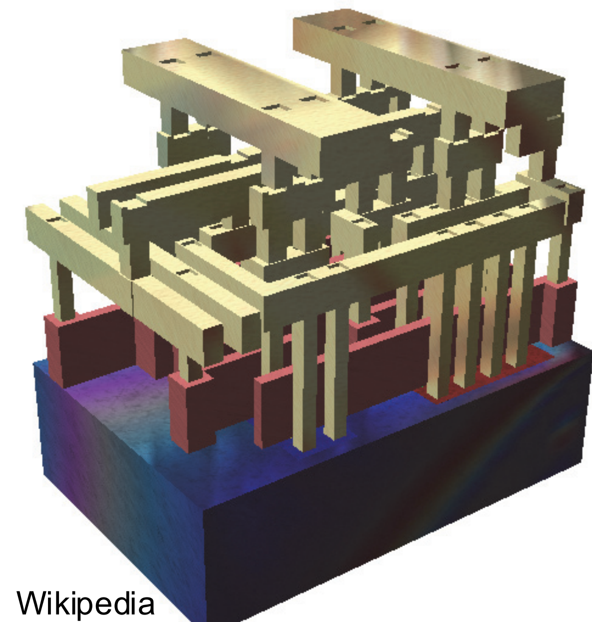

AMD

Brown University



Robert Richmond, 2003

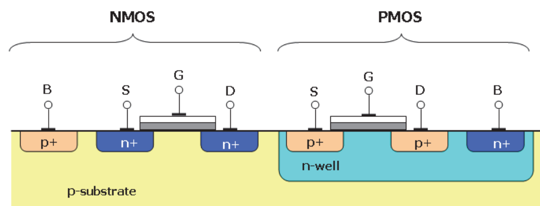



Wikipedia

Process steps

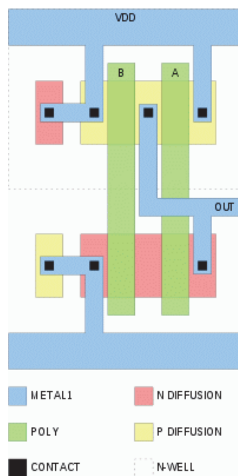
(2D-transistors)

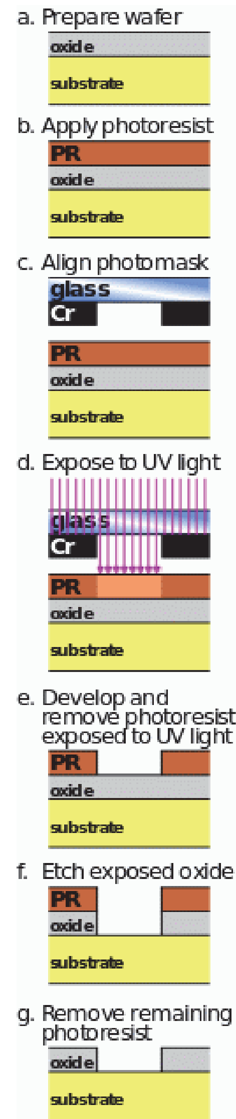
CMOS transitors (NOT-gate)



n – electrons (P, AS, Sb)
p – holes (B, Al)

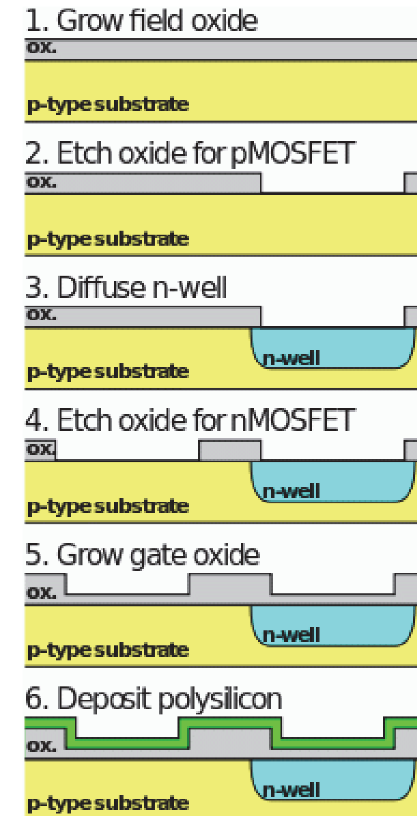
2-NAND layout

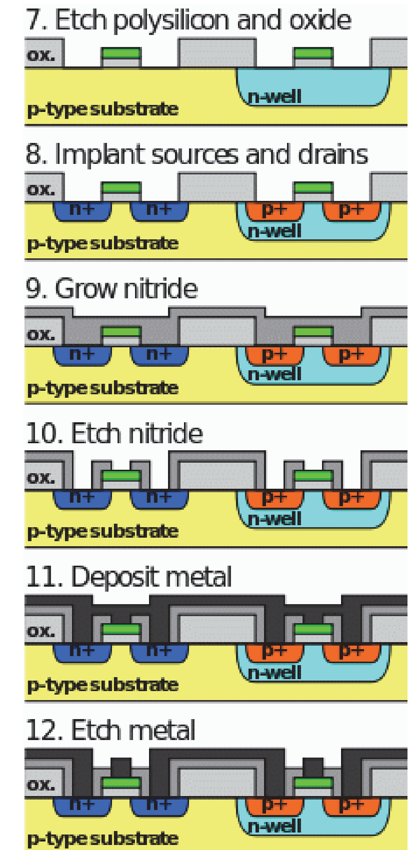




Etching steps

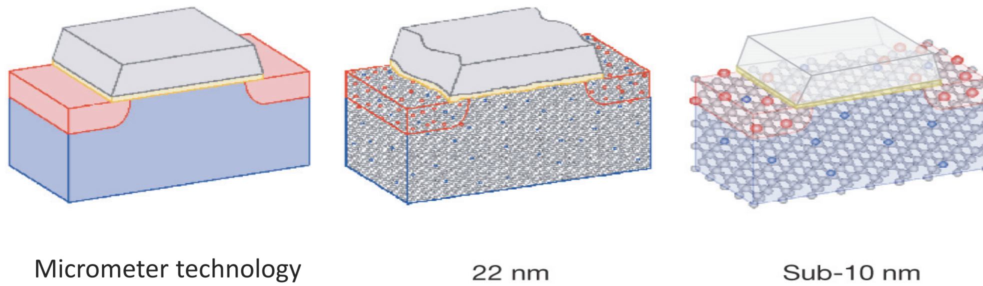
Process steps





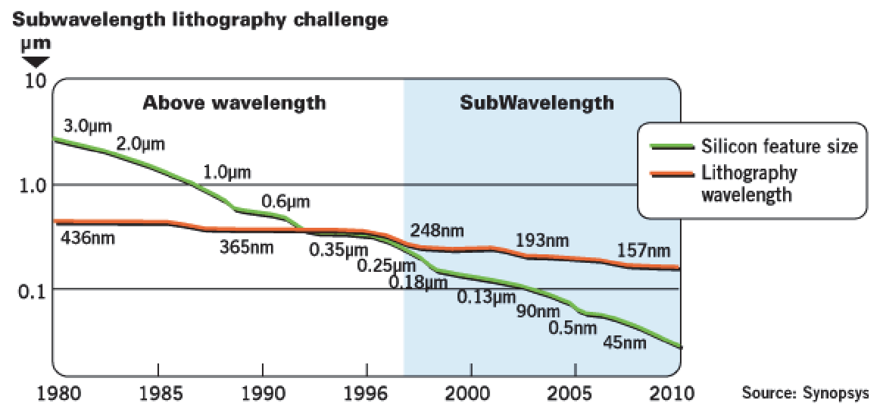
www.wikipedia.org

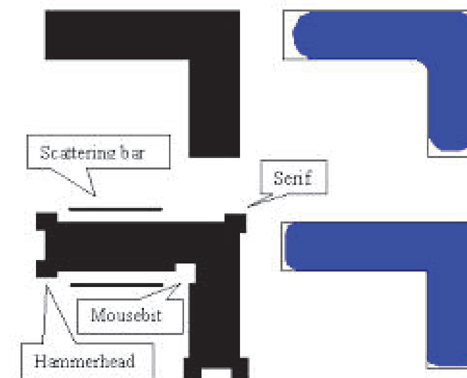
Miniaturization creates challenges



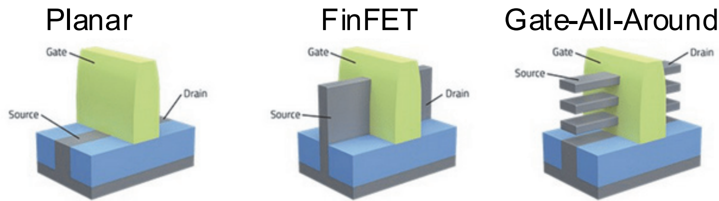
Photolithographic process

- Features smaller than the wavelength of light!!!!



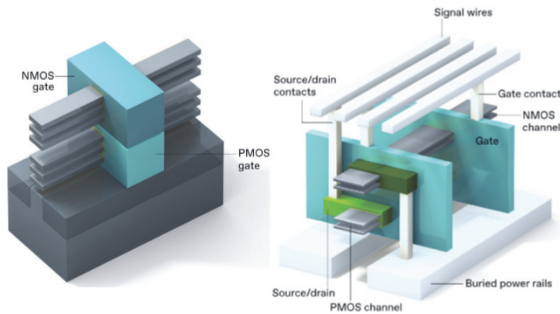


Sub-micron technologies (3D-transistors)



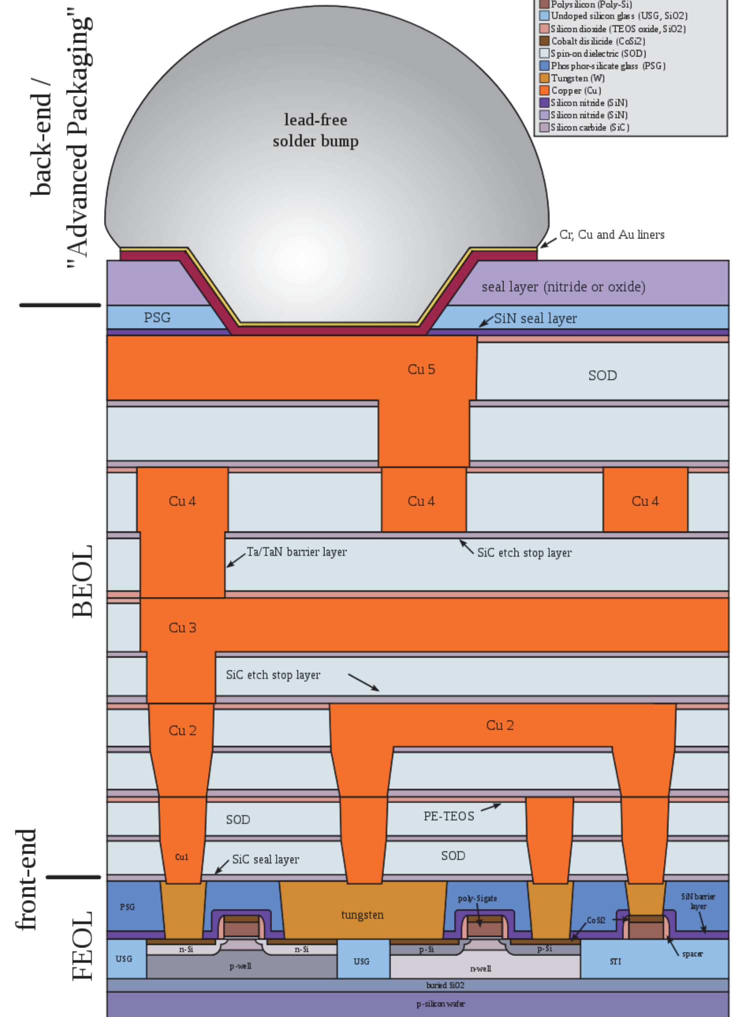
https://semiengineering.com/whats-after-finfets/

Transistors

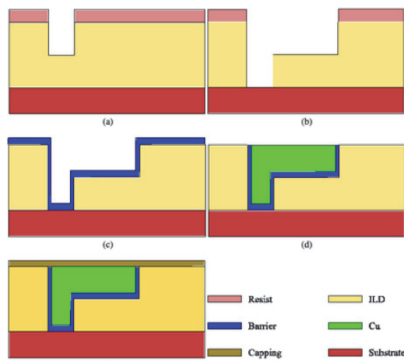


IEEE Spectrum 2022/12:
The Transistor at 75:
Taking Moore's Law to
New Heights [pp.32-37]

www.wikipedia.org



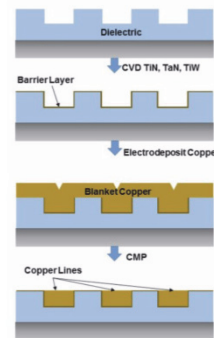
Dual-damascene fabrication process



https://picture.iczhiku.com/weixin/message1614096684818.html

Wires

Chemical
Mechanical
Polishing in
Damascene
Process

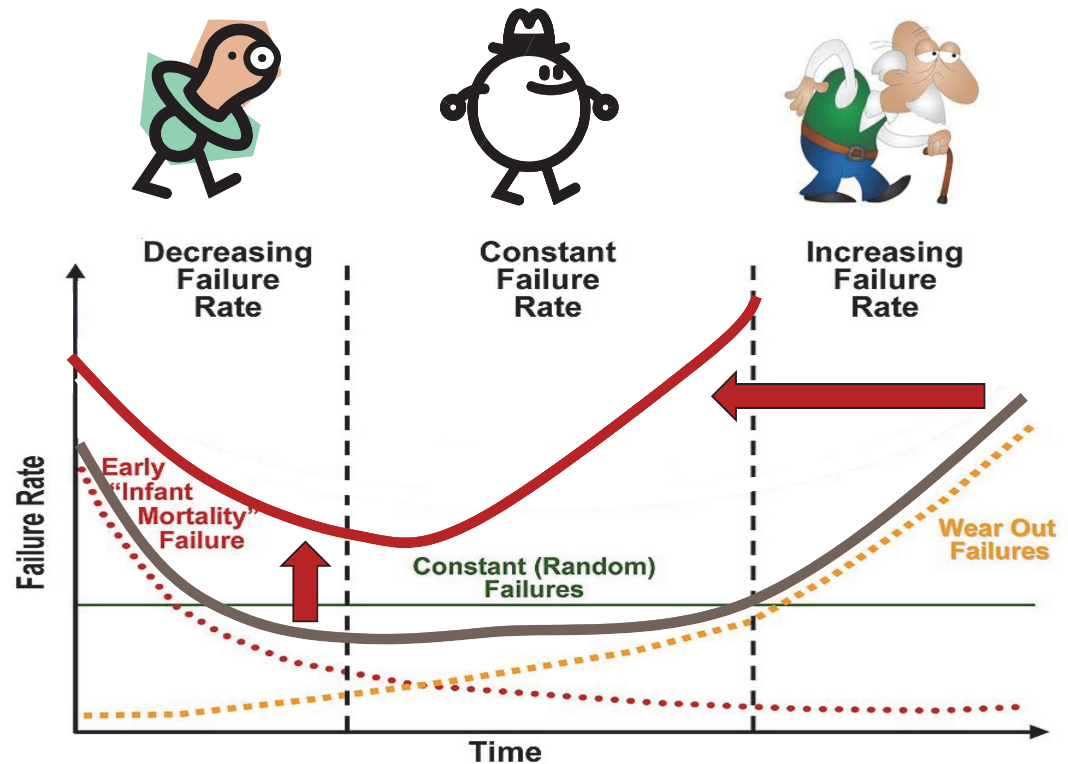


https://www.mks.com/n/chemical-mechanical-polishing

Challenges – failures

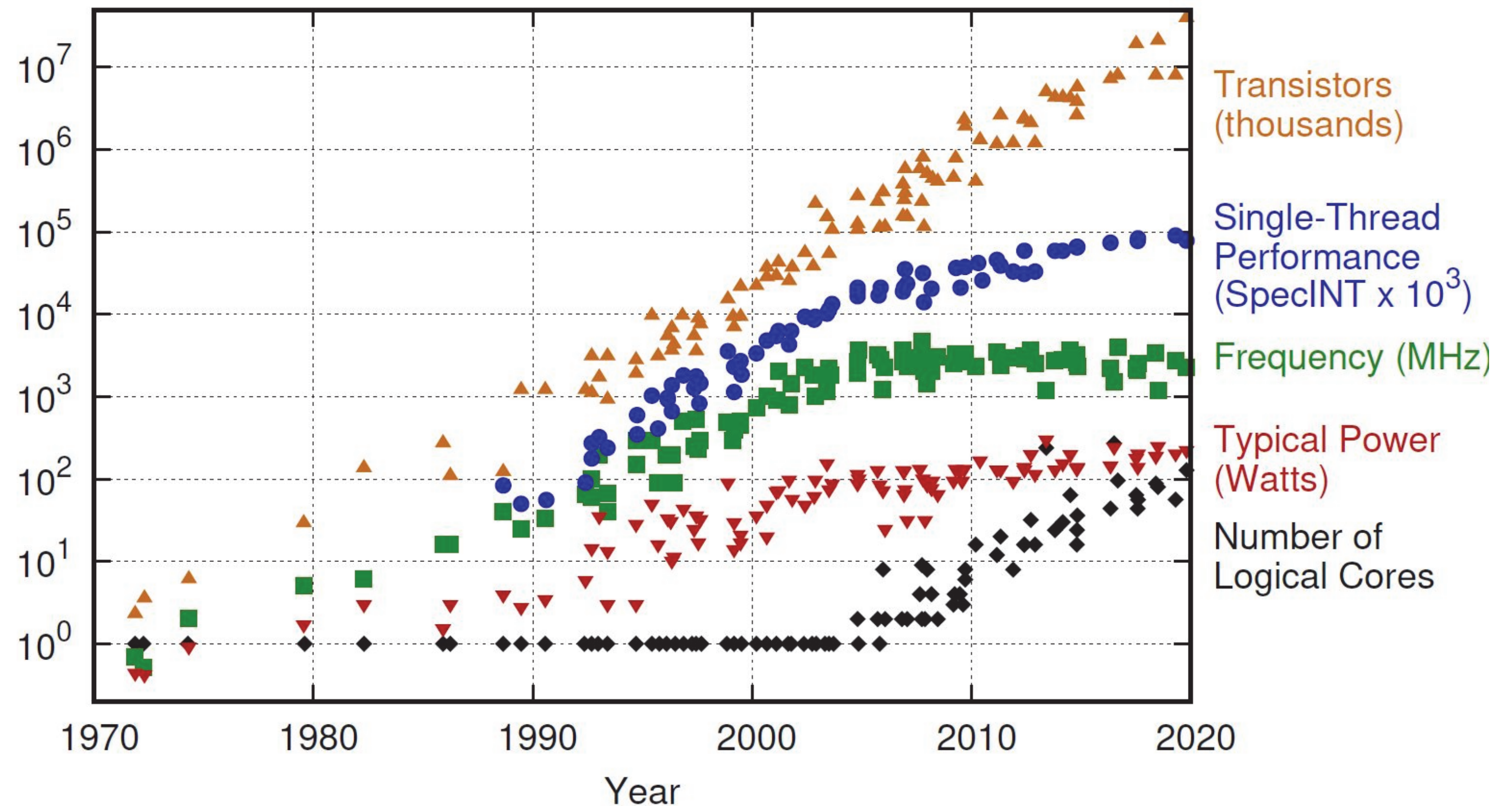
Rapidly increasing probability of failures

- Process variations
- Soft errors, EMC
- Aging phenomenon
  - NBTI (PBTI), Hot Carrier Injection, Electromigration



Challenges – energy density

Energy density is too high keep switching points cool!



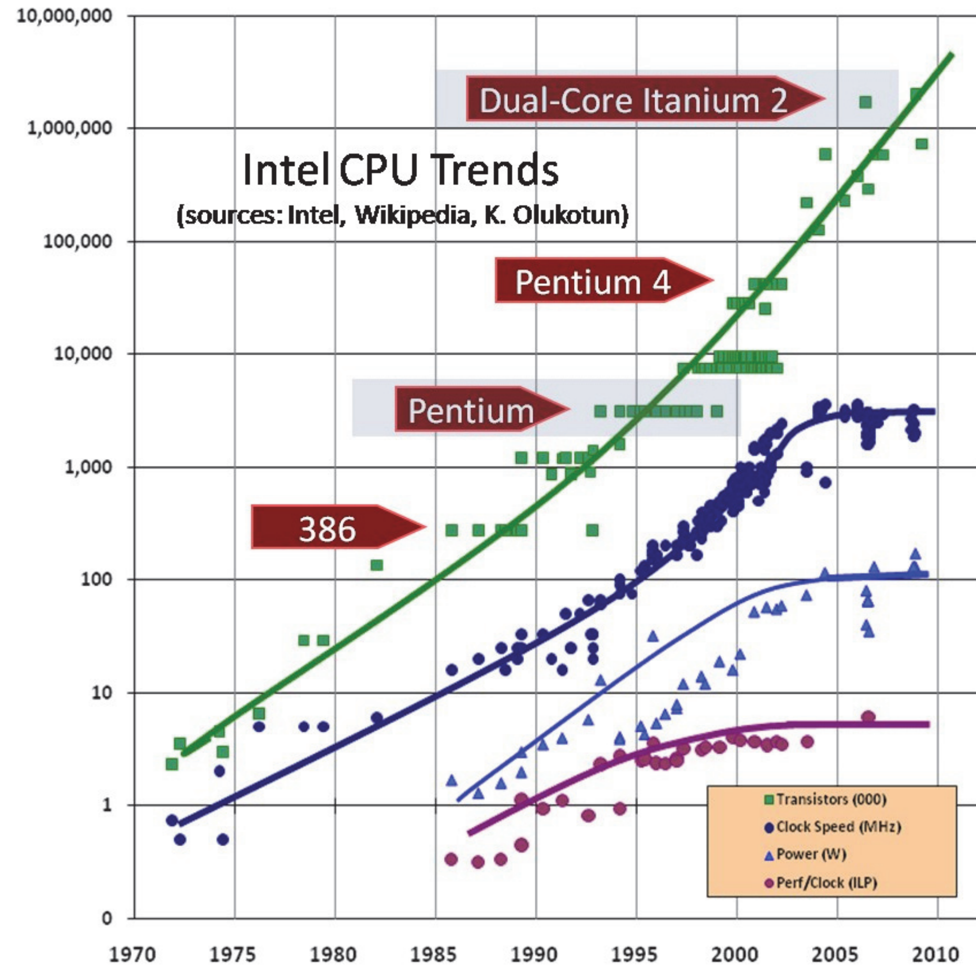
Trends so far…

	2000	2010	2020
memory size	2 Gbit	256 Gbit	1024 Gbit
transistors per cm^2	$8 \cdot 10^6$	$160 \cdot 10^6$	$480 \cdot 10^6$
internal clock frequency	1.5 GHz	10 GHz	40 GHz
external / bus clock frequency	0.5 GHz	1.5 GHz	2.5 GHz
pin count	2000	6000	10000
chip area	800 mm^2	1300 mm^2	1800 mm^2
wire width	140 nm	40 nm	10 nm
supply voltage	1.5 V	0.8 V	0.5 V
power consumption	100 W	170 W	300 W
power consumption (batteries)	0.5 W	1.5 W	2.5 W

NB! These are rough approximations only!

Trend toward multi-/many-core systems

1000s core processor chips in 2020s

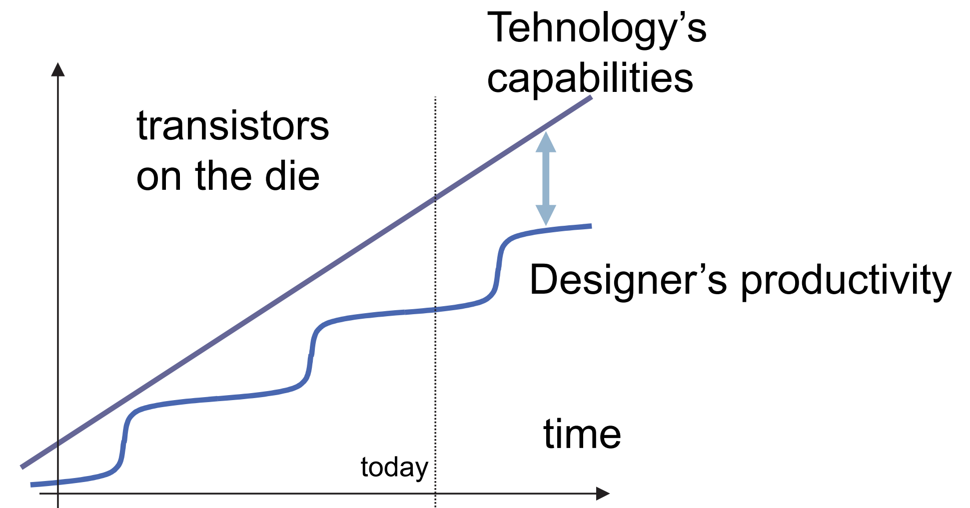


Challenges – design automation

Synthesis ~~ design automation

- 1990 – 4 Kgates / year / designer
- ...
- 2000 – synthesis (RTL–>GDSII) – 91K
- ...
- 2010 – homogeneous parallel
- processing (multi-core) – 1200K
- ...
- *Today – hw/sw co-verification, executable specification, etc.*

- productivity gap
    - 58% versus 21% annually



ASIC design process

S-1 Design Entry: Schematic entry or HDL description

S-2: Logic Synthesis: Using Verilog HDL or VHDL and Synthesis tool, produce ***a netlist***-logic cells and their interconnect detail

S-3 System Partitioning: Divide a large system into ASIC sized pieces

S-4 Pre-Layout Simulation: Check design functionality

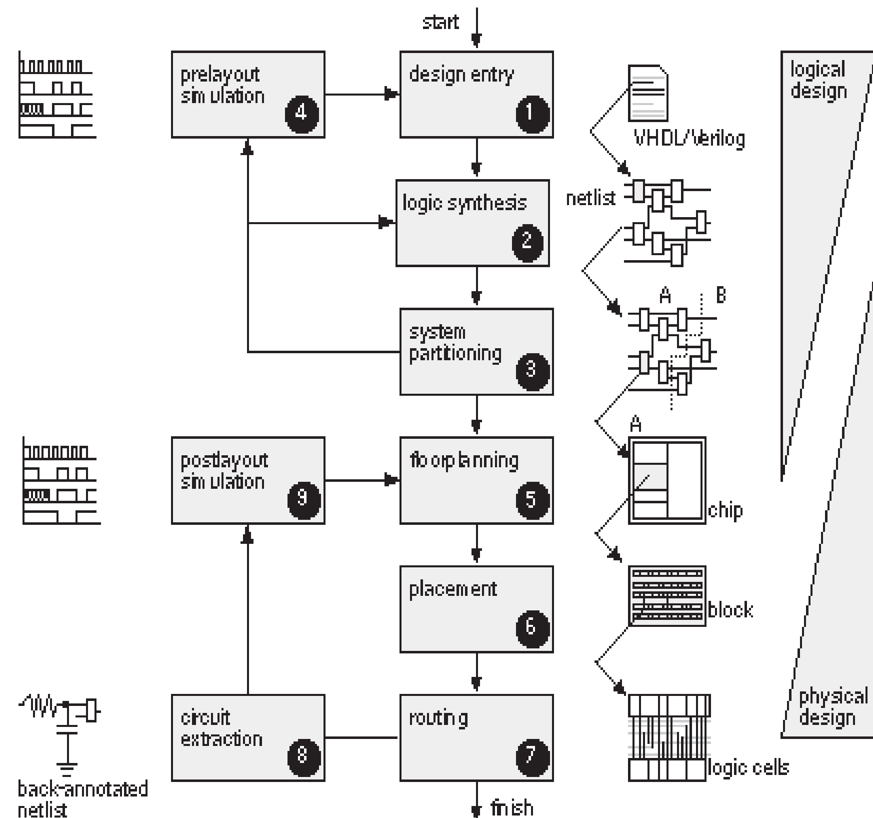
S-5 Floorplanning: Arrange netlist blocks on the chip

S-6 Placement: Fix cell locations in a block

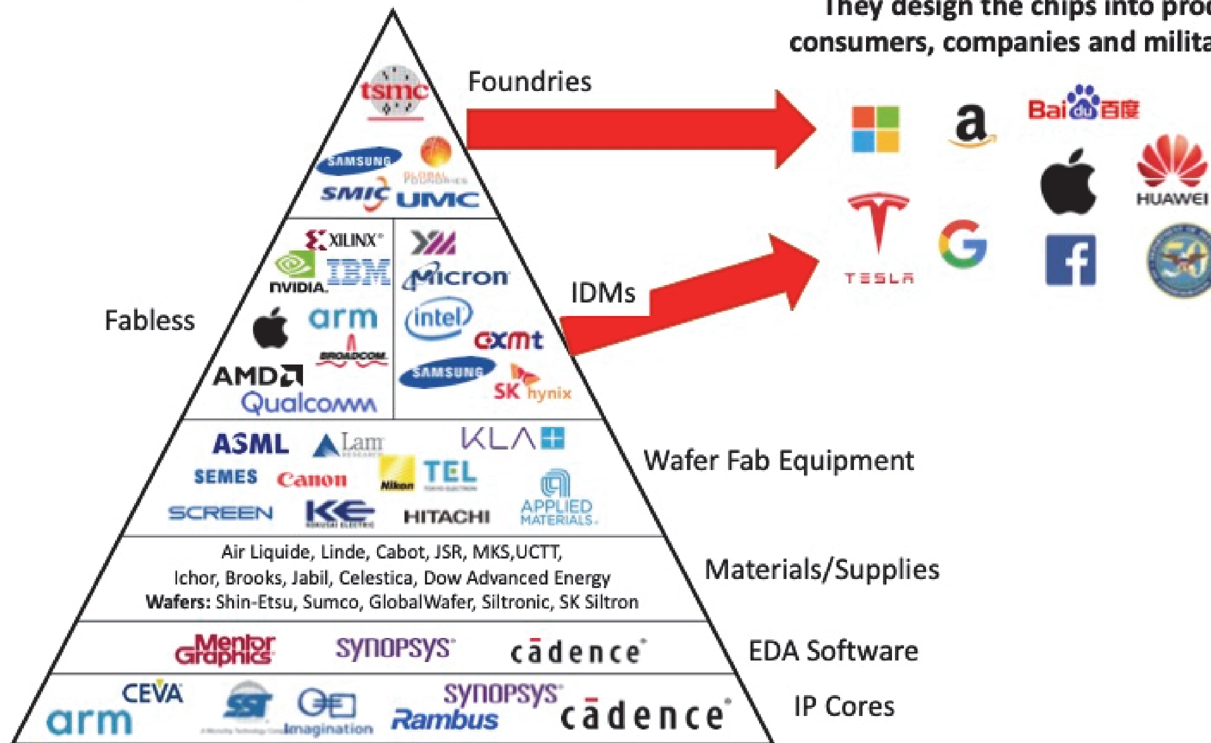
S-7 Routing: Make the cell and block interconnections

S-8 Extraction: Measure the interconnect R/C cost

S-9 Post-Layout Simulation



ASIC supply chain

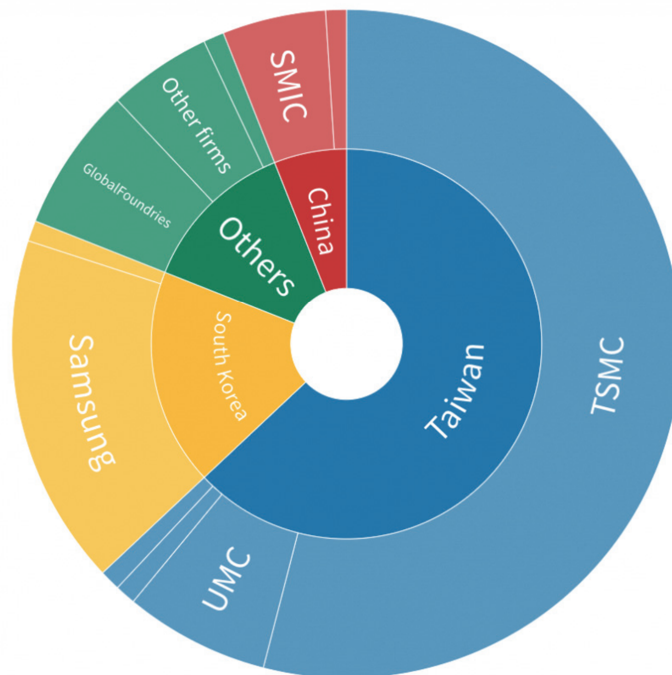


- Only 2-3 cutting-edge foundries
- + Only 2 IDMs (Integrated Device Manufacturers: Intel, Samsung
- + OSAT (Outsourced Semiconductor Assembly and Test)

ASIC foundries – Market share by countries

Semiconductor contract manufacturers by market share

Total foundry revenue stood at $85.13 billion in 2020



SOURCE: TrendForce (March 2021)

- More than 2/3 in Taiwan, mostly TSMC
- More than 90% in Asia

EU Chips Act

February 2022
#EUChipsAct #DigitalEU

Our aim is to jointly create a state-of-the-art European chip ecosystem, including production. We need to link together our world-class research, design and testing capacities. We need to coordinate EU and national investment along the value chain. This is not just a matter of our competitiveness. This is also a matter of tech sovereignty.

Ursula von der Leyen
President of the European Commission, 2021 State of the Union address

Semiconductor chips are the essential building blocks of digital products we use constantly ranging from smartphones and computers, to appliances in our homes, lifesaving medical equipment, communication, energy, industrial automation etc. Chips are everywhere.

In 2020, more than **1 trillion microchips** were manufactured around the world, about **130 chips for every person on earth**.

World shortage since 2020

Higher prices

Lengthier delivery for consumer electronics and life-saving equipment

Car production **decreased by 1/3** in some EU countries

Europe is strong in some specific areas

Semiconductor research
World leading techniques behind most advanced chips

Chip manufacturing equipment
central equipment for all advanced chips

Silicon wafers
mirror-like material essential for manufacturing semiconductors

Chips for automotive and for industrial equipment
EU companies global leaders on the market

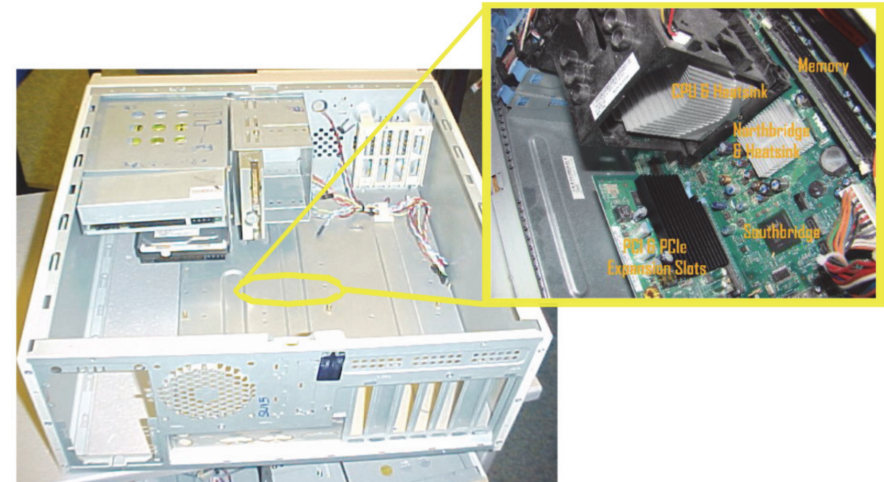
However, **the EU has only roughly 10% of global market share** and is heavily dependent on third-country suppliers.

The EU aims to play a leading role in the design and manufacturing of the next generation of microchips, down to 2 nanometers nodes and below. A nanometer is how much a fingernail grows per second.

Current state of art in chips: engraving at 5 nanometres

2022: 3 nanometres semiconductor goes into production. . . . . 2 nanometres and below are expected in **2024**.

Packaging issues



Mechanical requirements and constraints

- size, interfaces
- durability – dust, vibration

Thermal requirements and constraints

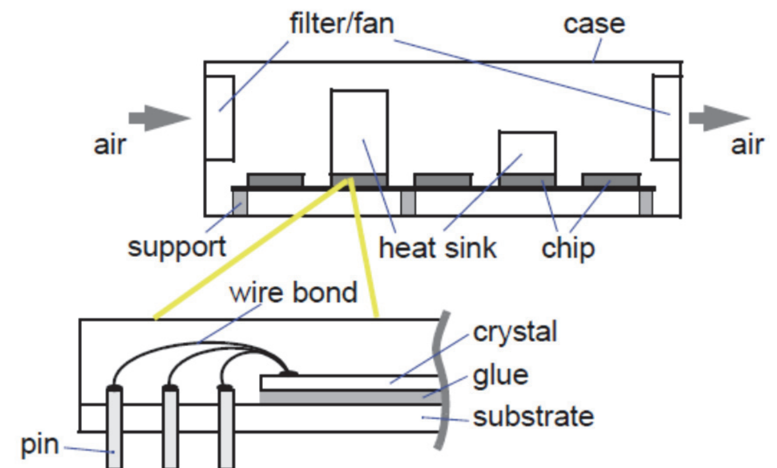
- work temperature range
- cooling / heating

Electrical requirements and constraints

- power supply
- protection – voltage, electromagnetic fields

Ergonomic requirements and constraints

- appearance, user interface, noise

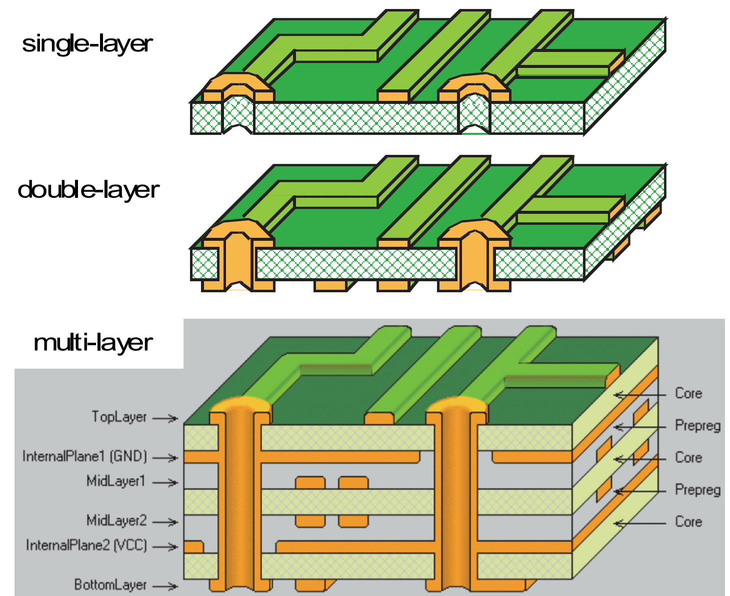


PCB – Printed Circuit Board

- Components
  - chips, transistors, resistors, capacitors, etc.
- Connections / interfaces / mounting

- PCB manufacturing
- Component placement (and fixing)
- Electrical connections (e.g. soldering)

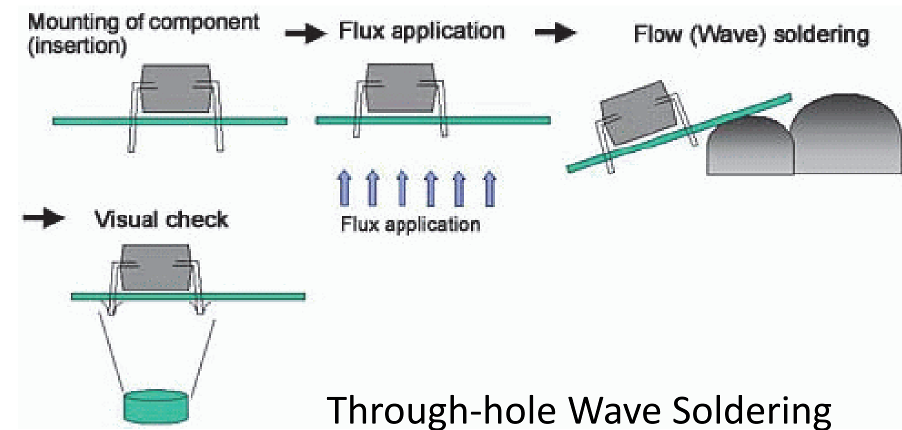
- Single-layer PCB
  - wires (bottom side)
- Double-layer PCB
  - wires + metallized vias
- Multi-layer PCB
  - multiple double-layer PCB-s
  - location of vias!



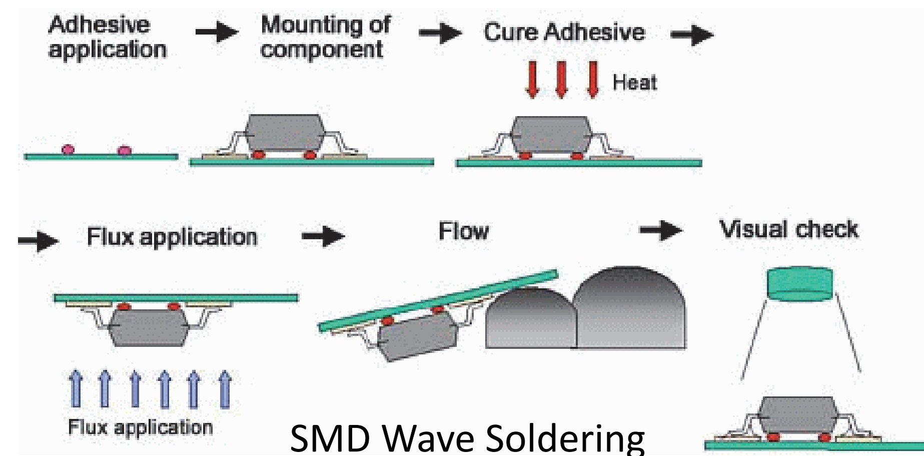
PCB manufacturing

Manufacturing

- component mounting
- soldering
  - solder paste / tin
- thermal problems
  - large copper surfaces
  - component over-heating
- quality check
  - visual inspection
- final finish
  - cleaning
  - protective lacquering
- final test
  - functional test



Through-hole Wave Soldering



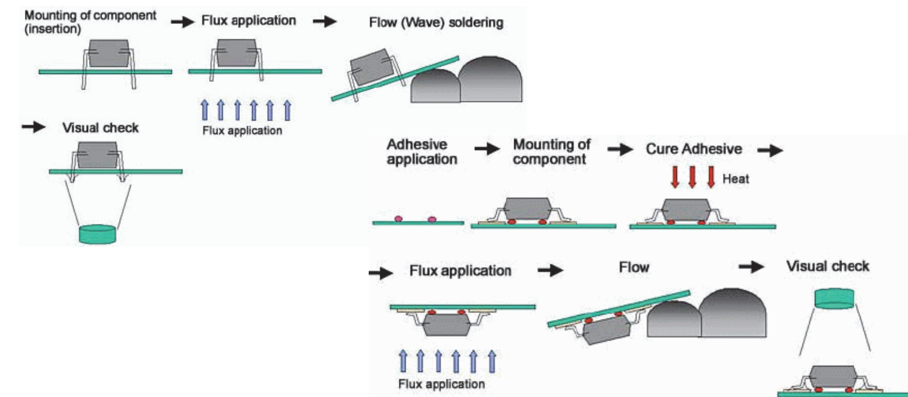
SMD Wave Soldering

PCB manufacturing

Wave Soldering

Electro Soft Inc.
https://www.youtube.com/watch?v=inHzaJIE7-4

Agrowtek Inc.
https://www.youtube.com/watch?v=VWH58QrprVc



SMD Reflow Soldering

GIGABYTE factory tour
https://www.youtube.com/watch?v=Va3Bfjn4inA

Tutorial
https://www.youtube.com/watch?v=gu0v8lfLcKg

SMD reflow at home
https://www.youtube.com/watch?v=U48Nose31d4