IAS0600 Digital Systems Design with VHDL

Course overview

Autumn, 2024

Course staff

• Lecturer

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- ICT-526

• Lab instructors

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Time and space – lectures and labs together

• Class

- ICT-501
- Use your Uni-ID to log in

• Time

- Wednesday
- 16:00-19:15
- Moodle page
 - Search for IAS0600 Digitaalsüsteemide disain VHDL-s (2024)
 - Enrollment key: (no key)
- Grading labs 70% + exam 30%
 - Detailed lab points distribution follows

Software and hardware

• Xilinx Design Software

- Vivado Design Suite (7-Series and newer)
 - Vivado ML Edition 2022.1 (in the lab)
 - Standard edition is free

• FPGA boards

- Digilent Nexys-4 DDR (Xilinx Artix-7 FPGA)
 - 18 boards
 - Used for labs 1–5

• QuestaSim (Mentor Graphics) & DesignVision (Synopsys)

• FIR design using High-Level Synthesis approach (Lab 6)

Digilent Nexys-4 DDR (Xilinx Artix-7 FPGA)



Installing Vivado on your own PC

- Create Xilinx account
- Make sure that you have 40+ Gb of free space
- Download installation files (Windows or Linux)

https://www.xilinx.com/support/download.html

- Select required features
 - Design Tools => Vivado Design Suite => Vivado
 - Devices => 7-Series => Artix 7
 - Installation Options => Install Cable Drivers
- Detailed step-by-step guide can be found at

https://digilent.com/reference/programmable-logic/guides/installing-vivado-and-vitis NOTE: We don't need Vitis and Vitis HLS

Lab syllabus

• Tutorial

• Half adder (introduction to Vivado)

• Regular labs

- Lab 1. Comparator
- Lab 2. Full adder
- Lab 3. Counter
- Lab 4. Creeping line
- Lab 5. Parameterizable Multiplier
- Lab 6. FIR Design & ASIC Synthesis (HDL & Synopsys)

Lab schedule

Tutorial

Week 2 (11.09)

Half adder

• Regular labs

Week 3 (18.09)	Lab 1. Comparator	5 points
Week 5 (02.10)	Lab 2. Full adder	5 points
Week 7 (16.10)	Lab 3. Counter	10 points
Week 9 (30.10)	Lab 4. Creeping line	10 points
Week 11 (16.11)	Lab 5. Multiplier	10 points
Week 13 (27.11)	Lab 6. FIR (HLS)	20+10 points

General lab requirements

- The deadline is the 16th week (20.12.2024), for Lab 6 exam date (TBD)
- Labs are done INDIVIDUALLY
- Labs are passed in the same order as they are listed in the schedule
- If the lab task consists of several steps, then each step requires a separate visual demonstration
- Each lab is meant to be completed within two weeks after the start date in the schedule
- For all questions/problems regarding the labs, please contact the lab staff

Lab submission

Step 1. Visual demonstration

- Checked during the lab
- Code, simulation waveform, on-board deployment

• Step 2. Defense

• Answer questions regarding the lab topic, design sources, etc.

• Step 3. Report

- Submit to Moodle
- Report (.pdf) + project archive (for Lab 6 report and design source files)
- Wait for acknowledgment of acceptance
- Should be submitted within 2 weeks after the lab is done

Report

The goals of the report

- Document the workflow
- Describe the results and their significance
- Demonstrate writer's comprehension
- Prove understanding of the topic

• Expected structure of the report

- Introduction
- Background
- Workflow
- Results and discussion
- Conclusion
- References and appendices

General report requirements

- Lab report should feature things that are specifically required to be included in the task
 - Answers to the questions
 - Figures, tables, Boolean equations, graphs, etc.
- Functional simulation should always be performed and described
 - If the results were checked automatically, describe how
 - If the results were checked manually, include meaningful screenshot(s) of the waveform and explain how did you verify that the design works correctly
- All objects in the text should be numbered, labeled, and referenced
- All figures, tables, code listings, statements, results should be explicitly explained within the text
- Do not put full source code in the report (it should be in the project archive)
- All materials taken from external sources should be referenced (also within the text)