### **Starting Cadence:**

- 1. open terminal window (command line)
- 2. type 'cad'
- 3. type 'cad' again
- 4. select 'O' as for 0) Old legacy CAD versions selection..
- 5. select '0' as for 0) CADENCE 2009/2010 IC/SYS combined with AMS designkit v3.70

For 'cold start' enter 'ams\_cds -tech cxq -mode fb'

For restarting just use 'ams\_cds'

Check if 'Library Manager' window is listing 'HRDLIB' and your own libraries (if any).

#### **Creating your own library:**

Select '**File**'  $\rightarrow$  '**New library**' and enter a new name for your library. Check 'Don't need a techfile' in following dialog window and click 'OK'.

Now you can start creating your own schematic by selecting your library and then selecting 'File'  $\rightarrow$  'New cellview'. Enter name for your schematic (keep view name as 'schematic'!).

After this, a schematic entry window will appear.

# Tools for schematic entry:

	Virtuoso® Schematic Editing: cadtest cadtest schematic	• =	×
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Tools	Design Window Edit Add Check Sheet Options Migrate		Help
I	- Check (design rules) & save		· · ·
٠	- Save		
€ <sup>2</sup>	- Zoom in (also mouse wheel)		· · ·
ସ୍	- Zoom out (also mouse wheel)		
Jr.	- Move component		
$\overset{\otimes}{\gg}$	<ul> <li>Copy component (select first)</li> </ul>		
34	- Delete ( 'Del' )		
$\cap$	- Undo last action ( 'u' )		
	- Property editor		
ų	- New components ( 'i' )		
<b>_</b> ^	- Single signal wire ( 'w' and 's' for snap )		
• ٦	- Bus wire ( 'W' and 's' for snap )		
abc	- Signal name label (bus tapping)		
•D	- I/O markers		
C	<pre>mouse L: schSingleSelectPt() M: schHiMousePopUp() R: hiRepeat()</pre>		
	HIT-Kit: 3.70 Tech: cxx User: test		

## **General design flow:**

- place components. Leave space for wires, wire labels, I/O markers etc.
- place I/O markers
- place wires
- Check & save
- Export EDIF 200

Avoid moving components and wires after they have been placed. This can cause unexpected connections to appear.

Use 'Esc' key to cancel current mode (wire, instance, delete etc).

### **Component selection:**

Open '**Instance**' menu, click '**Browse**', select **HRDLIB**, check '**Show Categories**'. In this lab, all components (except your own macros) come from HRDLIB. Select desired logic gate. Put window focus on Virtuoso Schematic Editing window and place the component.

Note that your components can be grouped like single wires in a bus:

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The latter is achieved by visiting '**Properties**' and adding <0:3> to '**Instance Name**' field:

		Edit Object P	roperties		+ = ×				
ОК	Cancel Apply	Defaults Prev	ious Next		Help				
Apply To Show	Apply To only current instance Show system User CDF								
	Browse	Reset Inst	ance Labels Di	splay					
	Property		Value		Display				
	Library Name	HRDLIE			off 🖃				
	Cell Name	INI	INI						
	View Name	symbolį			off =				
	Instance Name	, I1<0:3>			value 🗆				
		Add	Delete	Modify					

Same notation ise used everywhere else - wire labels, I/O pins. On the slide below there is an 4-bit Input pin named X and Output pin named Y. Using '**Wire Name**' tool, a single signal X<1> is taken out of the 4-bit bus. This signal drives inverter I0 and goes to I/O pin 'z'.

				Virtuos	50® 50	hematio	Editing: cadtest cadtest schematic
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#### How to create macro (custom instance):

Check & save first, then, in 'Virtuoso Schematic Editing' open

'**Design**' → '**Create Cellview**' → '**From Cellview**'. This opens confirmation/check dialog box. Click 'OK'. Next comes 'Symbol Generation Options' – where you can check I/O pin placement and visibility. Default is normally OK, so click 'OK'.

Now a 'Virtuoso Symbol Editing' window opens. You can do your finishing touches there and save your symbol (it is save into your library). Now you can use it on higher level schematic.

In case you need to modify your lower level designs (especially if adding/removing I/O markers), you'll be asked to regenerate the symbols and fix higher level schematics.

#### **Exporting design:**

Make sure all is correct – do a 'Check & Save' for each macro and top level design.

Find 'icfb – Log:' window. Check for any error report regarding 'Check & Save'. If all is OK, you can continue by selecting:

'File'  $\rightarrow$  'Export'  $\rightarrow$  'EDIF 200...'

A tall window named '**EDIF 200 Out**' appears. Start by clicking '**Browse**' and select your top level design to be exported.

Set 'Design Name' field to something. It has to be filled, although its precise value doesn't actually matter much.

Set 'External Libraries' and 'Stop Cell Expansion File' to HRDLIB.

Try setting '**Output Format**'  $\rightarrow$  '**Netlist**' and '**Netlist TranslationMode**'  $\rightarrow$  '**Flat**'. If exporting fails see error messages. You may need to set the latter to 'Hierarchical'.

Look at 'icfb – Log:'. During EDIFOUT there should be no mention of **pmos** and **nmos**. If there is, check if above fields are filled in correctly.

	EDIF 200 Out	+ @ ×
OK Cancel Defa	ults Apply	Help
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	Load Save	
Design	Browse	
Run Directory	- The second sec	
Library Name	cadtest	
Cell Name	cadtest	
View Name	schematic	
External Libraries	HRDLIE	
Design Name	test	
User-Defined SKILL File	Į.	
Hierarchy File	Yes H	
Stop Cell Expansion File	HRDLIE	
Output File	edif.outi	
Technology File	default.tf	
Output CDF Data ?	◆ No	
	Ves, as properties in the outputed EDIF file	
	V res, w seperate cui uata mes	
ReplaceBundleWithArray	◆ TRUE ◇ FALSE	
Output Format	🔷 Schematic 🔶 Netlist	
Generate Scalar EDIF	◆ FALSE ◇ TRUE	
	Evnand All Objects	
	<ul> <li>Expand All Objects</li> <li>Expand All Objects Except Ports</li> </ul>	
Inherited Connections	<ul> <li>Use Default Value (Ignore Expressions)</li> <li>Interpret Expressions</li> </ul>	
NetlistTranslationMode	🔷 Hierarchical 🔶 Flat	

## **Obtaining printout:**

First, copy a plotter setup file to your home root directory: **cp** ~/**M**/**Elmet.Orasson/.cdsplotinit** ~/

Place a frame around the schematic you want to print, these come from '**US\_8ths**'. Save design. In 'Virtuoso Schematic Editing' open 'Design'  $\rightarrow$  'Plot'  $\rightarrow$  'Submit' dialog.

In 'Submit Plot' dialog, uncheck 'Plot With' → 'header' option and go on to '**Plot Options ...**'

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OK Canc	el Defaults App	ly	Help						
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	Fu	l Size Sele	ct						
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Plotter Name	LaserJet								
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Plot To File	Not Selected		The Low Key						
			Plot Options						

In 'Plot Options' select 'Center Plot' & 'Fit to Page', 'Send Plot Only To File', uncheck 'Mail Log To'. Don't forget to fill plot file name field!

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Resulting file should be a PostScript file which can be converted into PDF (using **ps2pdf** command line utility) format or even be included in report directly.