Starting Cadence:

1. open terminal window (command line)
2. type '**cad**'
3. type '**cad**' again
4. select '**0**' as for `0) Old legacy CAD versions selection..`
5. select '**0**' as for 0) CADENCE 2009/2010 IC/SYS combined with AMS designkit v3.70

For 'cold start' enter '**`ams_cds -tech cxq -mode fb`**'

For restarting just use '**`ams_cds`**'

Check if 'Library Manager' window is listing '**HRDLIB**' and your own libraries (if any).

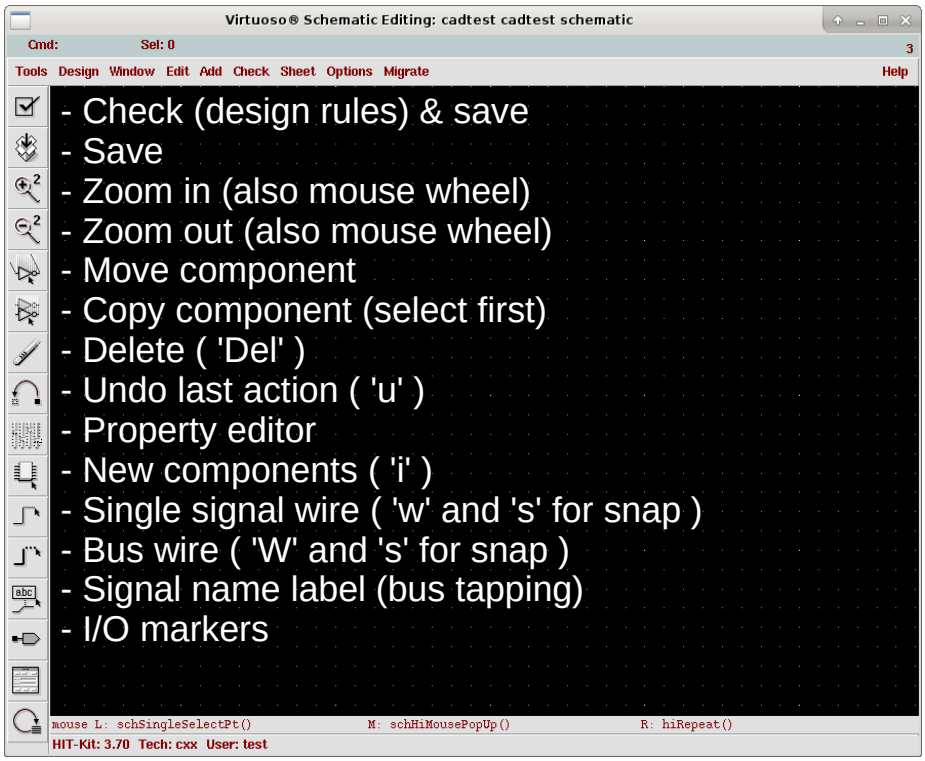
Creating your own library:

Select '**File**' → '**New library**' and enter a new name for your library. Check 'Don't need a techfile' in following dialog window and click 'OK'.

Now you can start creating your own schematic by selecting your library and then selecting '**File**' → '**New cellview**'. Enter name for your schematic (keep view name as 'schematic'!).

After this, a schematic entry window will appear.

Tools for schematic entry:



General design flow:

- place components. Leave space for wires, wire labels, I/O markers etc.
- place I/O markers
- place wires
- Check & save
- Export EDIF 200

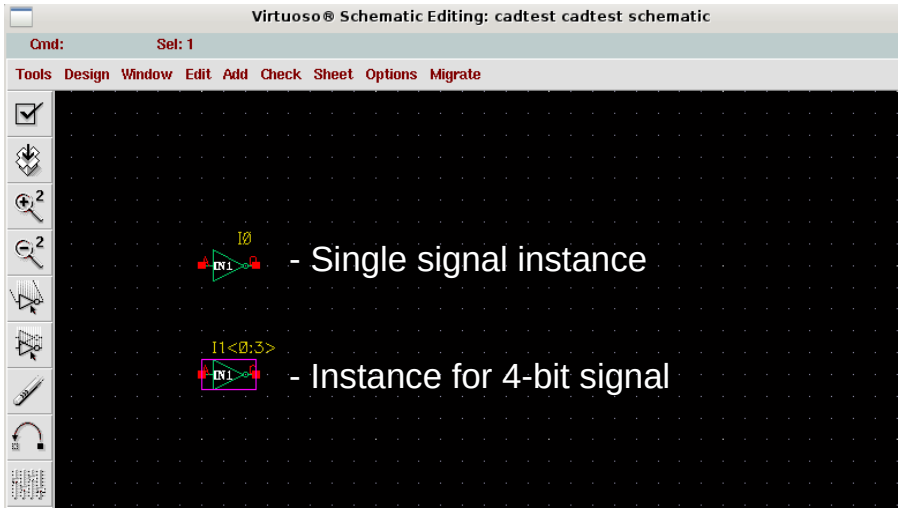
Avoid moving components and wires after they have been placed. This can cause unexpected connections to appear.

Use '**Esc**' key to cancel current mode (wire, instance, delete etc).

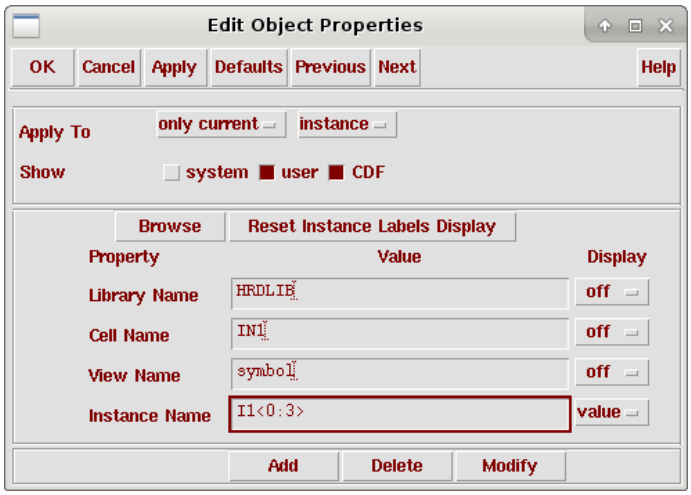
Component selection:

Open '**Instance**' menu, click '**Browse**', select **HRDLIB**, check '**Show Categories**'. In this lab, all components (except your own macros) come from HRDLIB. Select desired logic gate. Put window focus on Virtuoso Schematic Editing window and place the component.

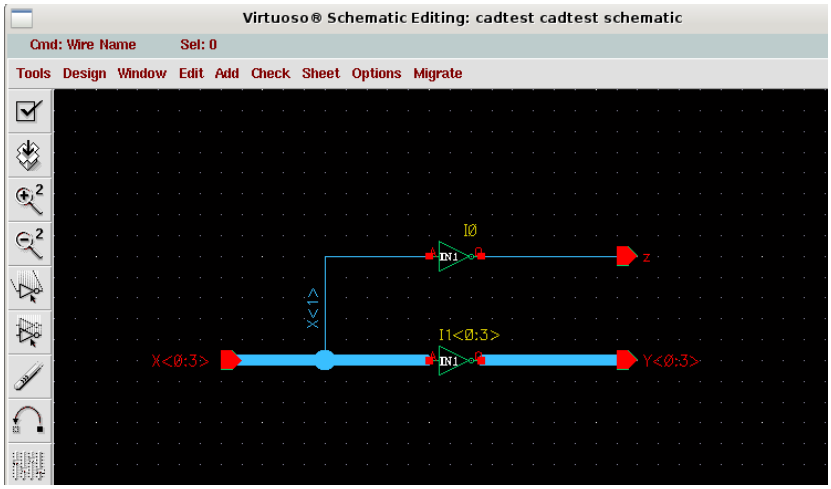
Note that your components can be grouped like single wires in a bus:



The latter is achieved by visiting '**Properties**' and adding <0:3> to '**Instance Name**' field:



Same notation ise used everywhere else - wire labels, I/O pins. On the slide below there is an 4-bit Input pin named X and Output pin named Y. Using '**Wire Name**' tool, a single signal X<1> is taken out of the 4-bit bus. This signal drives inverter I0 and goes to I/O pin 'z'.



How to create macro (custom instance):

Check & save first, then, in 'Virtuoso Schematic Editing' open
'**Design**' → '**Create Cellview**' → '**From Cellview**'. This opens confirmation/check dialog box. Click 'OK'. Next comes 'Symbol Generation Options' – where you can check I/O pin placement and visibility. Default is normally OK, so click 'OK'.

Now a 'Virtuoso Symbol Editing' window opens. You can do your finishing touches there and save your symbol (it is save into your library). Now you can use it on higher level schematic.

In case you need to modify your lower level designs (especially if adding/removing I/O markers), you'll be asked to regenerate the symbols and fix higher level schematics.

Exporting design:

Make sure all is correct – do a 'Check & Save' for each macro and top level design.

Find 'icfb – Log:' window. Check for any error report regarding 'Check & Save'. If all is OK, you can continue by selecting:
'**File**' → '**Export**' → '**EDIF 200...**'

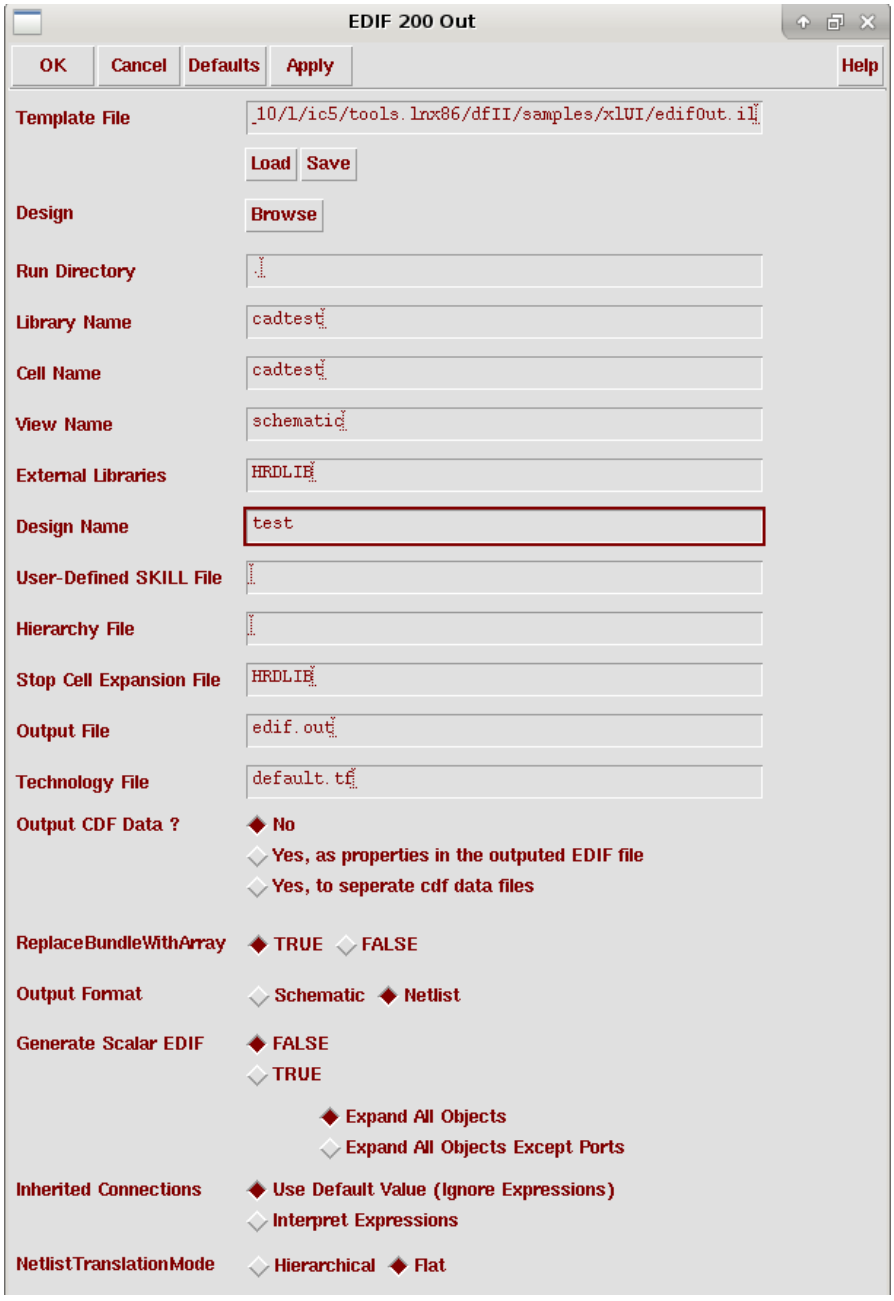
A tall window named '**EDIF 200 Out**' appears. Start by clicking '**Browse**' and select your top level design to be exported.

Set 'Design Name' field to something. It has to be filled, although its precise value doesn't actually matter much.

Set '**External Libraries**' and '**Stop Cell Expansion File**' to HRDLIB.

Try setting '**Output Format**' → '**Netlist**' and '**Netlist TranslationMode**' → '**Flat**'. If exporting fails see error messages. You may need to set the latter to 'Hierarchical'.

Look at 'icfb – Log:'. During EDIFOUT there should be no mention of **pmos** and **nmos**. If there is, check if above fields are filled in correctly.

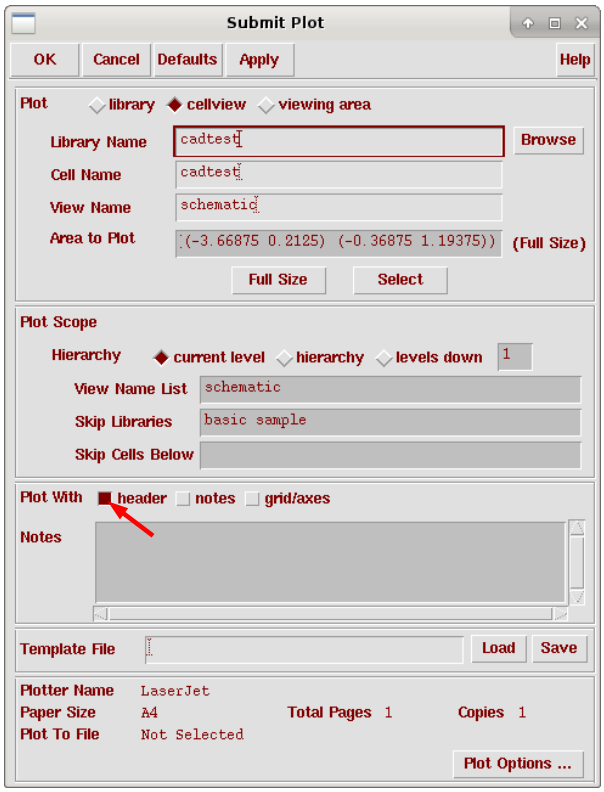


Obtaining printout:

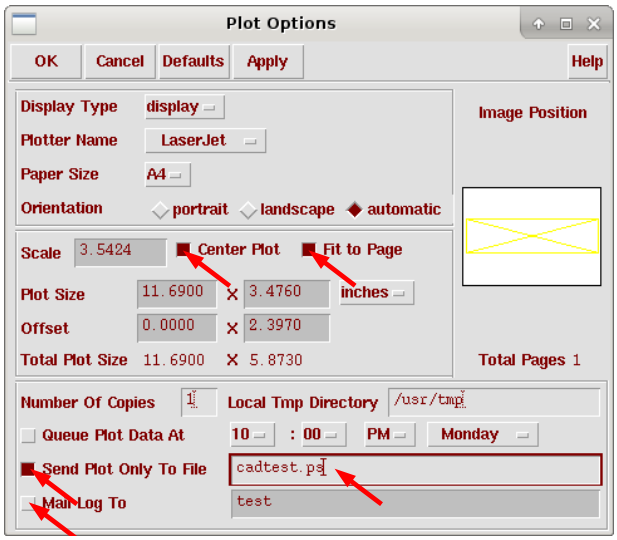
First, copy a plotter setup file to your home root directory:
cp ~/M/Elmet.Orasson/.cdsplotinit ~/

Place a frame around the schematic you want to print, these come from '**US_8ths**'. Save design. In 'Virtuoso Schematic Editing' open 'Design' → 'Plot' → 'Submit' dialog.

In 'Submit Plot' dialog, uncheck 'Plot With' → 'header' option and go on to '**Plot Options ...**'



In 'Plot Options' select 'Center Plot' & 'Fit to Page', 'Send Plot Only To File', uncheck 'Mail Log To'. Don't forget to fill plot file name field!



Resulting file should be a PostScript file which can be converted into PDF (using **ps2pdf** command line utility) format or even be included in report directly.